HUASHUO SEMICONDUCTOR

HSBA4909

N-Ch and P-Ch Fast Switching MOSFETs

Description

The HSBA4909 is the high performance complementary N-ch and P-ch MOSFETs with high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

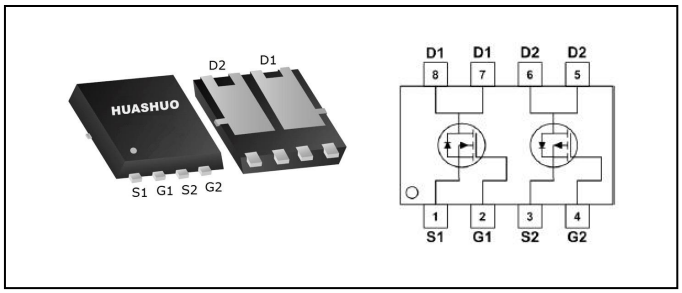
The HSBA4909 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Product Summary

BVDSS	RDSON	ID
40V	8mΩ	40A
-40V	13mΩ	-40A

PRPAK5*6 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	40	-40	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	28	-28	A
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	15	-15	A
I_D@T_A=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	10	-10	A
I_{DM}	Pulsed Drain Current[2]	120	-120	A
EAS	Single Pulse Avalanche Energy[3]	76	146	mJ
I_{AS}	Avalanche Current	39	-54	A
P_D@T_C=25℃	Total Power Dissipation[4]	36	36	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	62	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	3.5	℃/W

N-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	40	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.034	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=12A	---	---	8	mΩ
		V_{GS}=4.5V , I_D=10A	---	---	10	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.0	1.5	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.56	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=32V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=32V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}= ± 20V , V_{DS}=0V	---	---	± 100	nA
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.6	---	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=20V , V_{GS}=4.5V , I_D=12A	---	19	---	nC
Q_{gs}	Gate-Source Charge		---	4.7	---	
Q_{gd}	Gate-Drain Charge		---	8.5	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=3.3Ω I_D=1A	---	14.5	---	ns
T_r	Rise Time		---	2.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	77	---	
T_f	Fall Time		---	4.8	---	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	2333	---	pF
C_{oss}	Output Capacitance		---	176	---	
C_{rss}	Reverse Transfer Capacitance		---	136	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	15	A
I_{SM}	Pulsed Source Current[2,5]		---	---	39	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1	V

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=39A
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-40	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.012	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-8A	---	---	13	mΩ
		V_{GS}=-4.5V , I_D=-4A	---	---	20	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.0	-1.5	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.32	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-32V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=-32V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}= ± 20V , V_{DS}=0V	---	---	± 100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-18A	---	24	---	S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-20V , V_{GS}=-4.5V , I_D=-12A	---	29	---	nC
Q_{gs}	Gate-Source Charge		---	7.7	---	
Q_{gd}	Gate-Drain Charge		---	7.6	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V , V_{GS}=-10V , R_G=3.3Ω, I_D=-1A	---	40	---	ns
T_r	Rise Time		---	35	---	
$T_{d(off)}$	Turn-Off Delay Time		---	100	---	
T_f	Fall Time		---	9.6	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	3500	---	pF
C_{oss}	Output Capacitance		---	323	---	
C_{rss}	Reverse Transfer Capacitance		---	222	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	-15	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1	V

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-54A
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

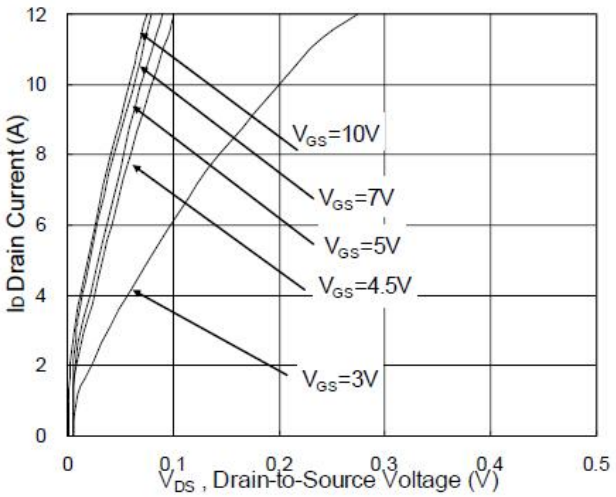


Fig.1 Typical Output Characteristics

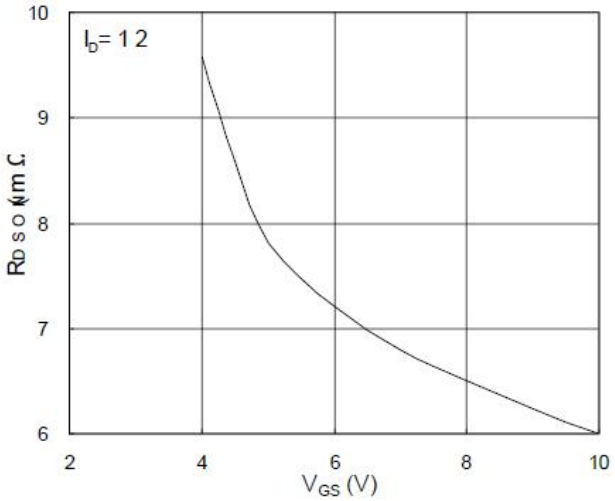


Fig.2 On-Resistance vs. G-S Voltage

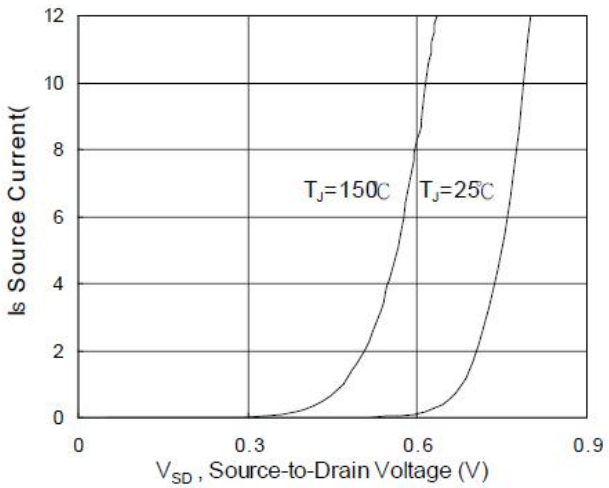


Fig.3 Forward Characteristics of Reverse

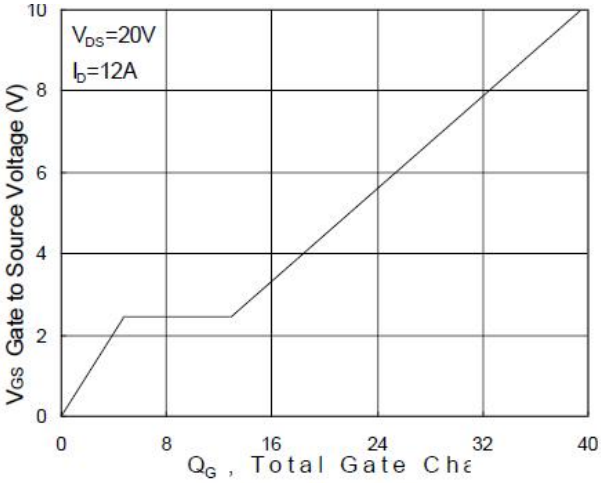


Fig.4 Gate-Charge Characteristics

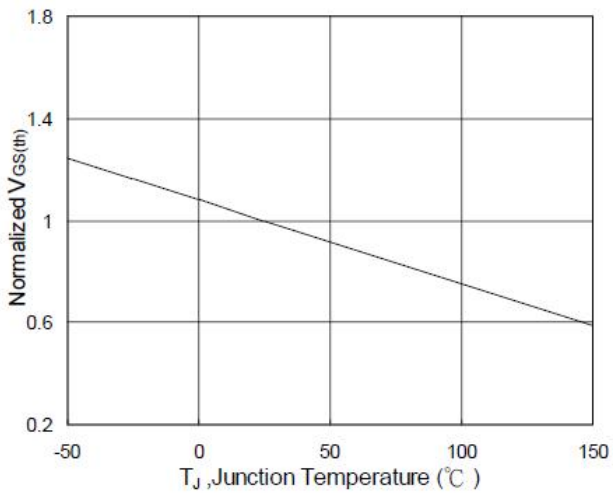


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

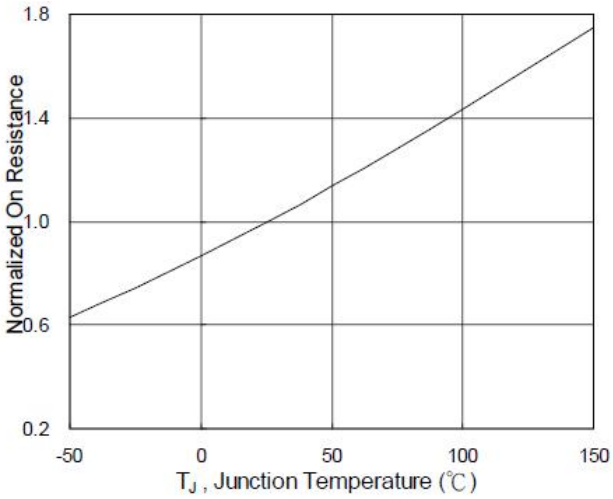


Fig.6 Normalized R_{DSON} vs. T_J

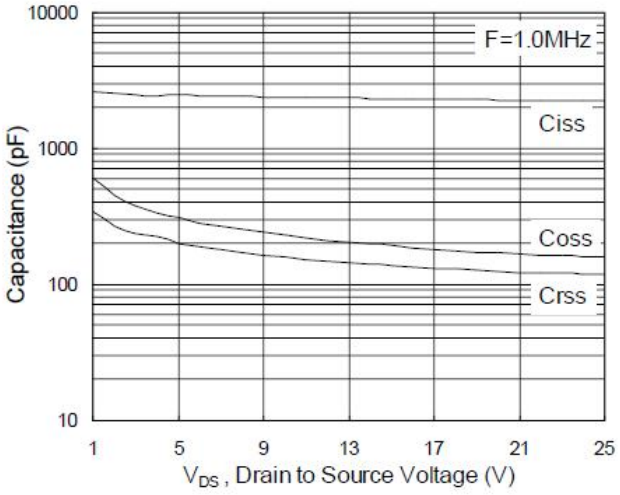


Fig.7 Capacitance

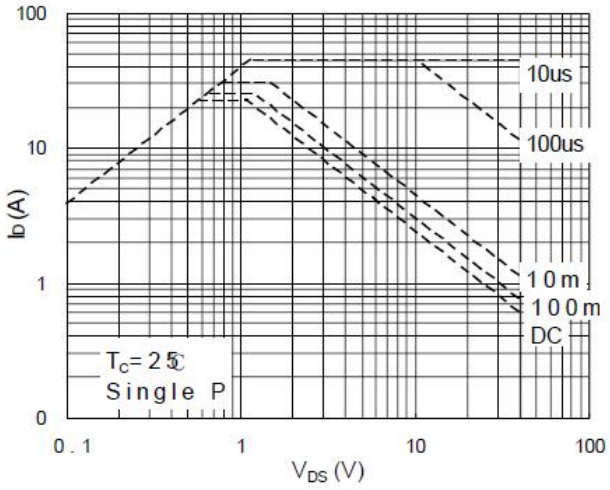


Fig.8 Safe Operating Area

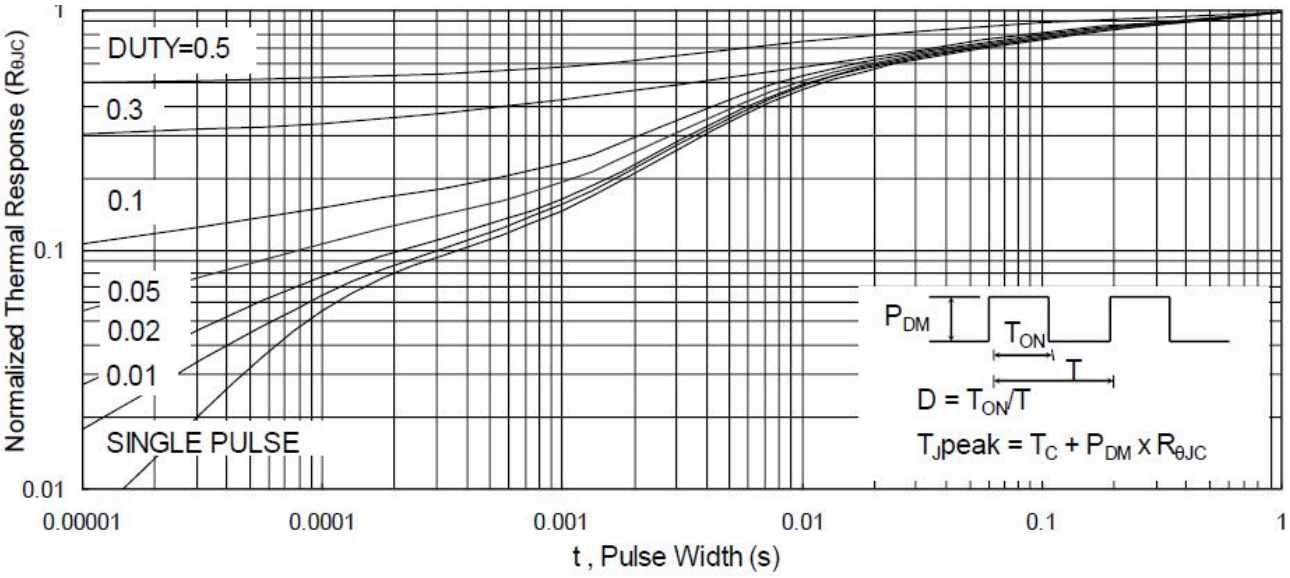


Fig.9 Normalized Maximum Transient Thermal Impedance

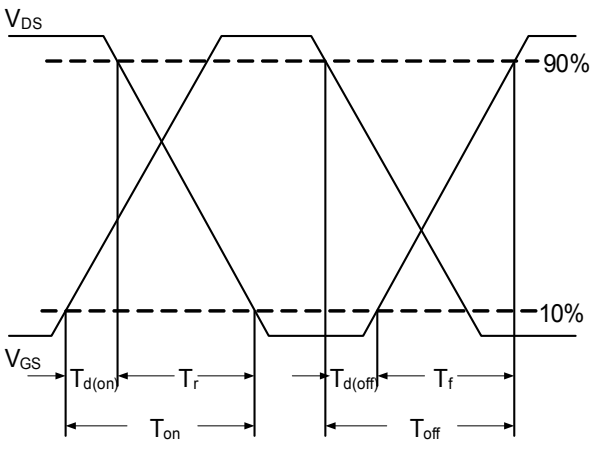


Fig.10 Switching Time Waveform

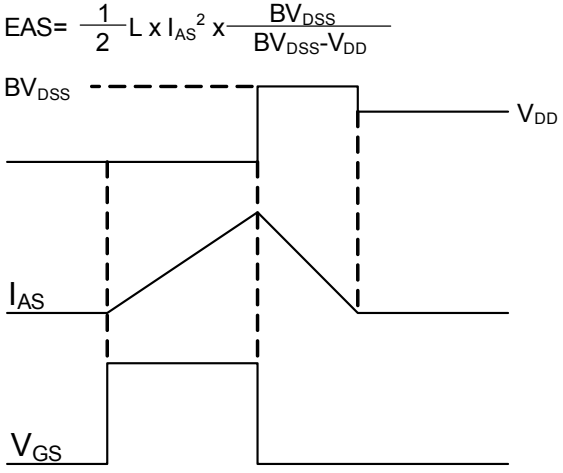


Fig.11 Unclamped Inductive Switching Wave

P-Channel Typical Characteristics

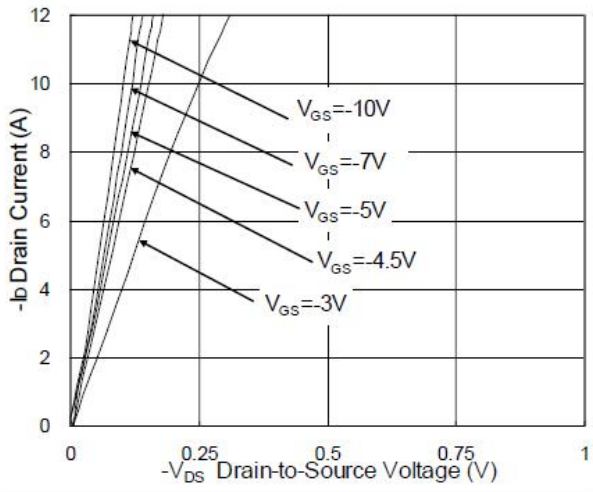


Fig.1 Typical Output Characteristics

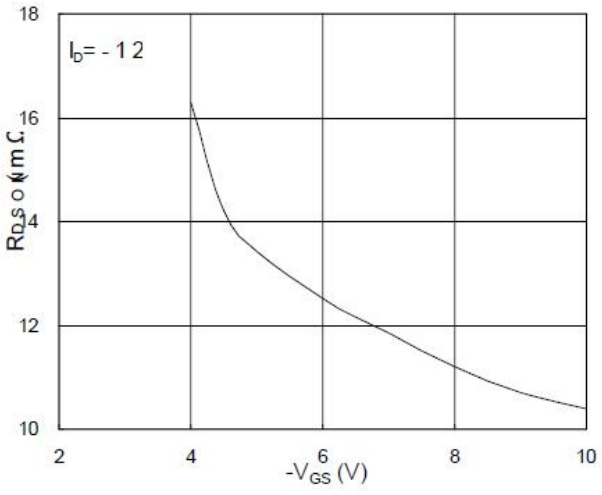


Fig.2 On-Resistance v.s Gate-Source

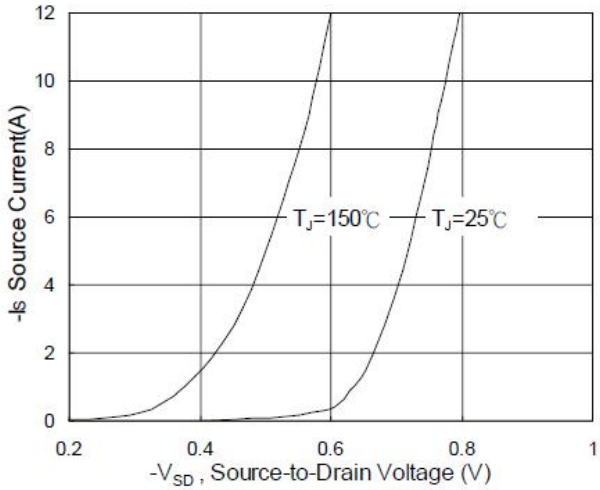


Fig.3 Forward Characteristics of Reverse

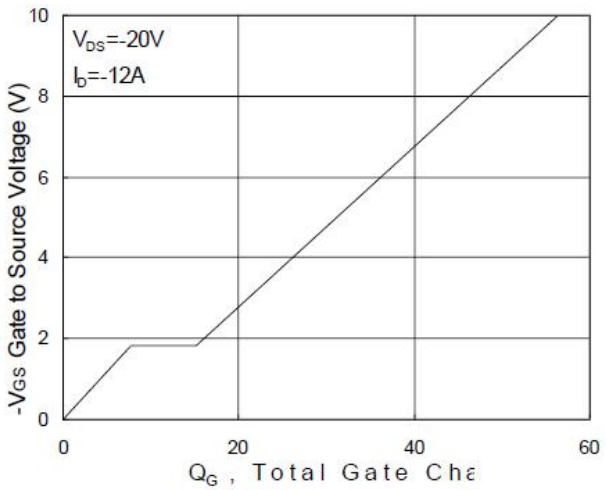


Fig.4 Gate-Charge Characteristics

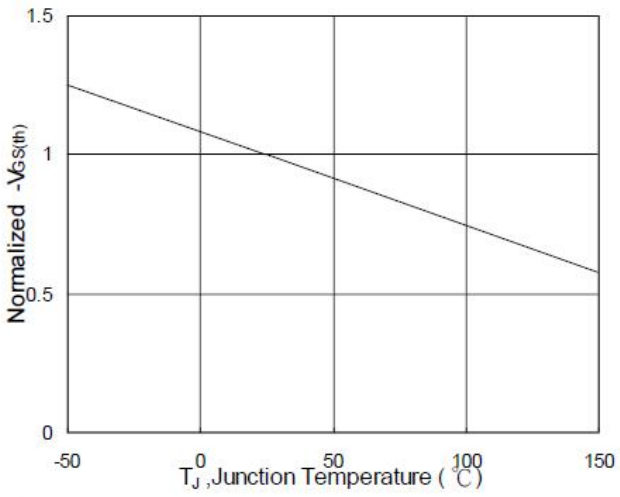


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

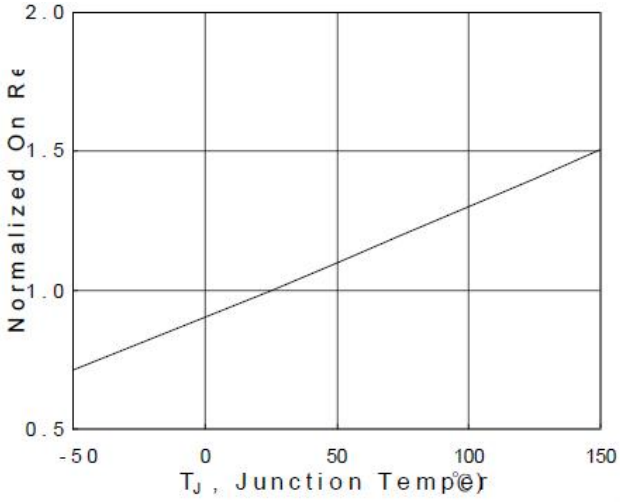


Fig.6 Normalized R_{DSON} v.s T_J

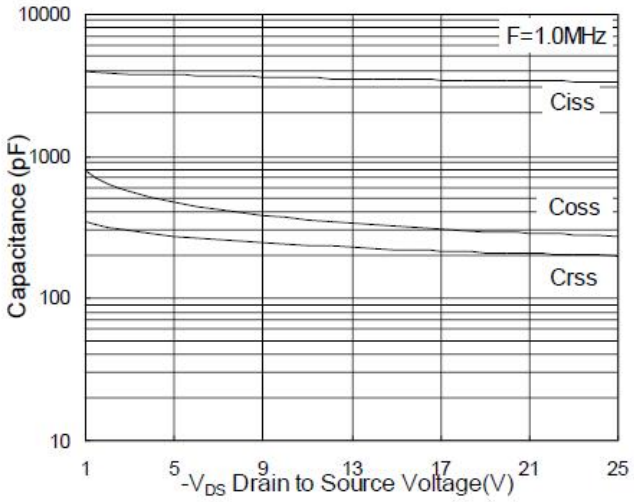


Fig.7 Capacitance

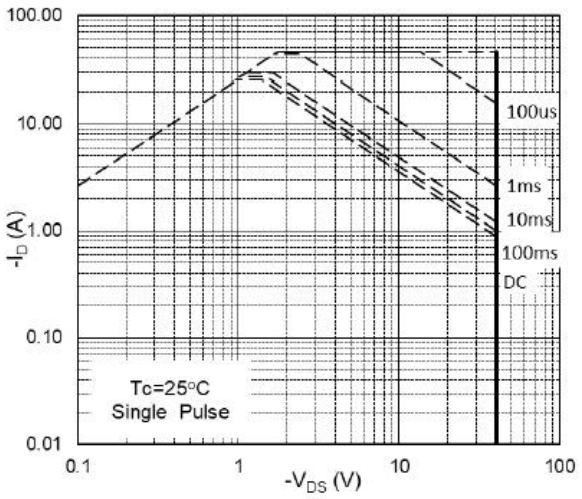


Fig.8 Safe Operating Area

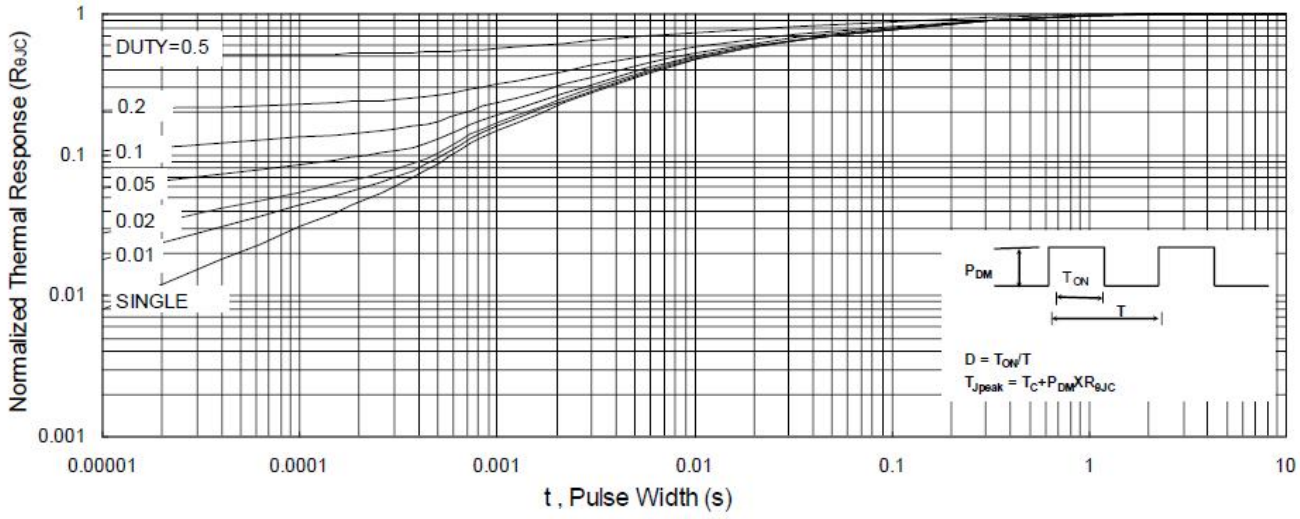


Fig.9 Normalized Maximum Transient Thermal Impedance

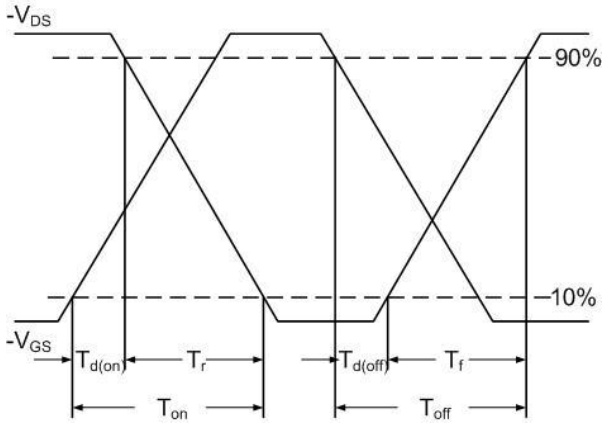


Fig.10 Switching Time Waveform

$$EAS = \frac{1}{2} L \times (-I_{AS}^2) \times \frac{-BV_{DSS}}{-BV_{DSS}-(-V_{DD})}$$

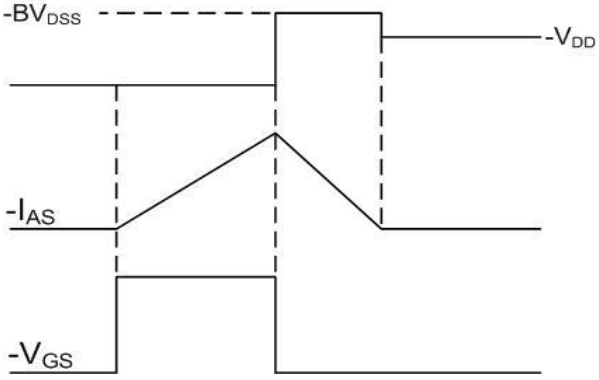
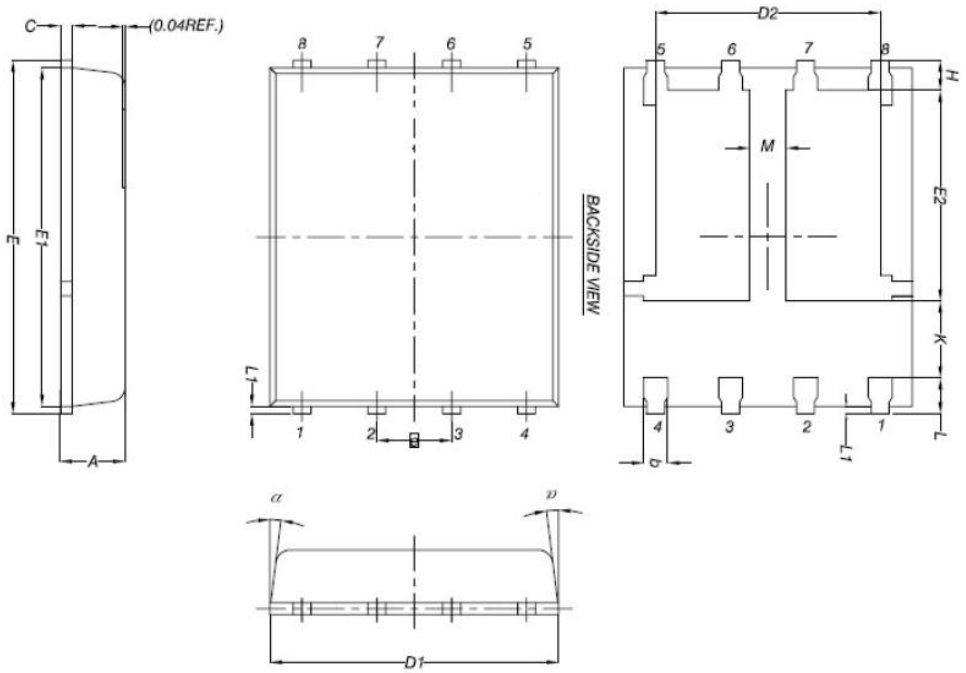


Fig.11 Unclamped Inductive Waveform

PRPAK5x6-8L Dual EP2 Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.17	0.035	0.046
b	0.33	0.51	0.013	0.020
C	0.20	0.30	0.008	0.012
D1	4.80	5.20	0.189	0.205
D2	3.61	3.96	0.142	0.156
E	5.90	6.15	0.232	0.242
E1	5.70	5.85	0.224	0.230
E2	3.30	3.78	0.130	0.149
e	1.27 BSC		0.05 BSC	
H	0.38	0.61	0.015	0.024
K	1.10	---	0.043	---
L	0.38	0.61	0.015	0.024
L1	0.05	0.25	0.002	0.010
M	0.50	---	0.020	---
α	0°	12°	0°	12°