



Description

- Proprietary New Trench Technology
- $R_{DS(ON),typ.} = 43m\Omega @ V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

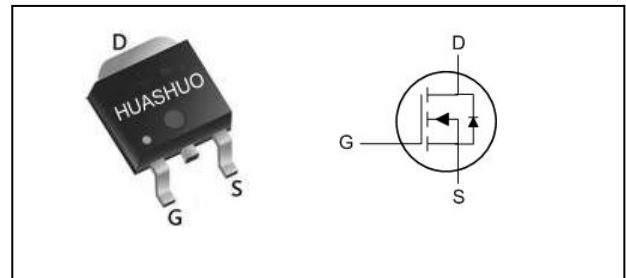
Product Summary

V_{DS}	200	V
$R_{DS(ON),max}$	48	m Ω
I_D	30	A

Applications

- Synchronous Rectification in SMPS
- Motor Control
- Hard Switching and High Speed Circuit

TO-252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	200	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	30	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	21	A
I_{DM}	Pulsed Drain Current ²	120	A
EAS	Single Pulse Avalanche Energy ³	200	mJ
dv/dt	Peak Diode Recovery dv/dt	5	V/nS
$P_D @ T_C=25^\circ C$	Total Power Dissipation ³	150	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	---	55	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	1.5	$^\circ C/W$



Electrical Characteristics ($T_J=25\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	200	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=20A$	---	42	48	m Ω
	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V, I_D=20A$	---	48	60	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	2.3	3.0	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=200V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=160V, V_{GS}=0V, T_J=125^\circ\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
Q_g	Total Gate Charge	$V_{DS}=100V, V_{GS}=10V, I_D=15A$	---	49	---	nC
Q_{gs}	Gate-Source Charge		---	11	---	
Q_{gd}	Gate-Drain Charge		---	8	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=100V, V_{GS}=10V, R_G=10\Omega$ $I_D=15A$	---	22	---	ns
T_r	Rise Time		---	5.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	75	---	
T_f	Fall Time		---	11	---	
C_{iss}	Input Capacitance	$V_{DS}=100V, V_{GS}=0V, f=1\text{MHz}$	---	3490	---	pF
C_{oss}	Output Capacitance		---	13	---	
C_{rss}	Reverse Transfer Capacitance		---	86	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	30	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	120	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=15A, dI/dt=100A/\mu s$, $T_J=25^\circ\text{C}$	---	117	---	nS
Q_{rr}	Reverse Recovery Charge		---	333	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150 $^\circ\text{C}$ junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Characteristics

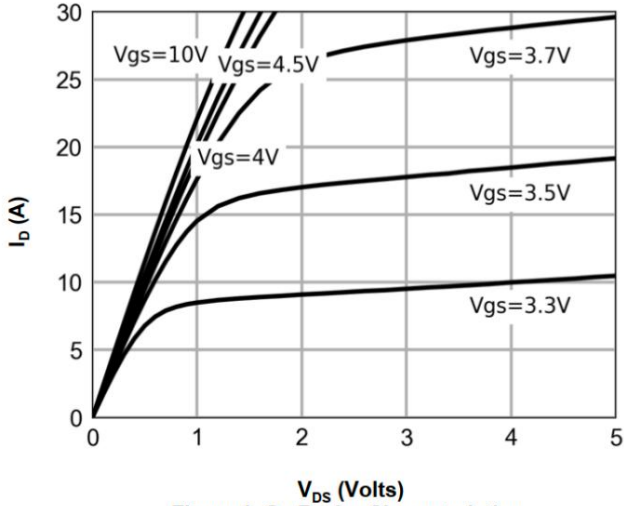


Figure 1: On-Region Characteristics

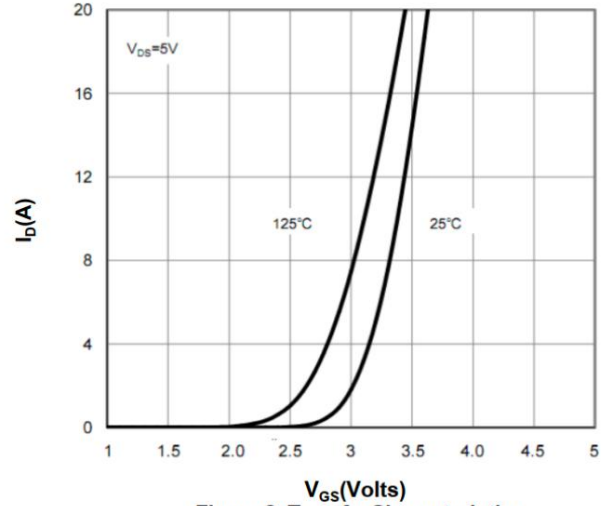


Figure 2: Transfer Characteristics

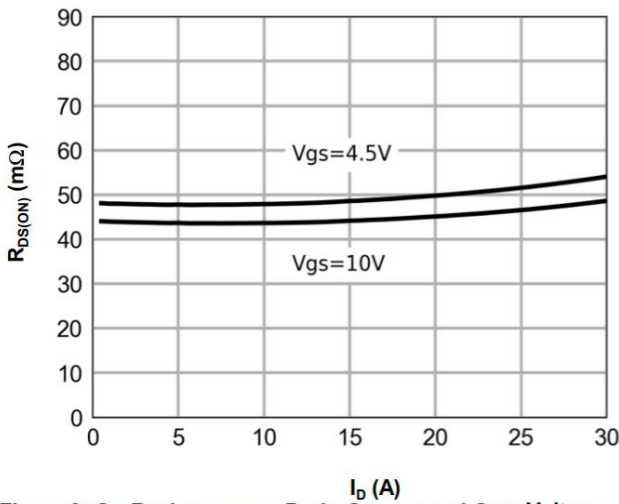


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

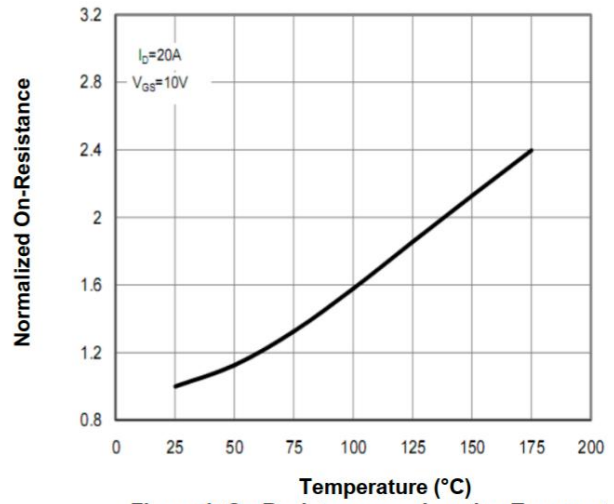


Figure 4: On-Resistance vs. Junction Temperature

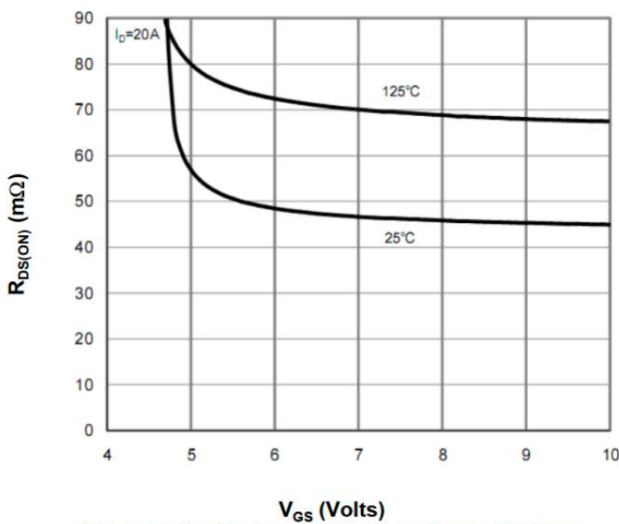


Figure 5: On-Resistance vs. Gate-Source Voltage

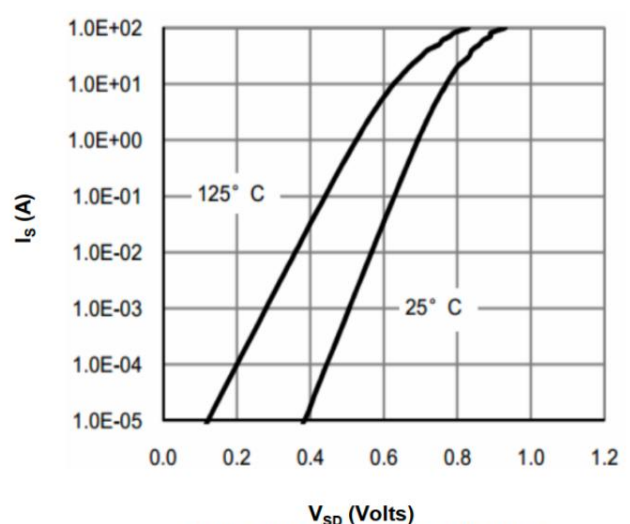


Figure 6: Body-Diode Characteristics

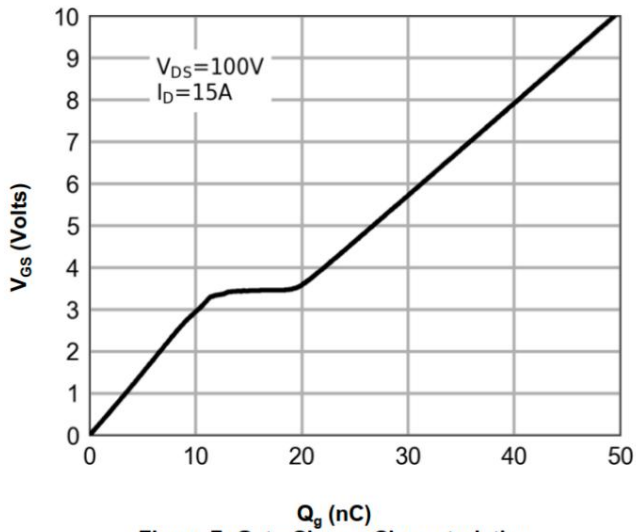


Figure 7: Gate-Charge Characteristics

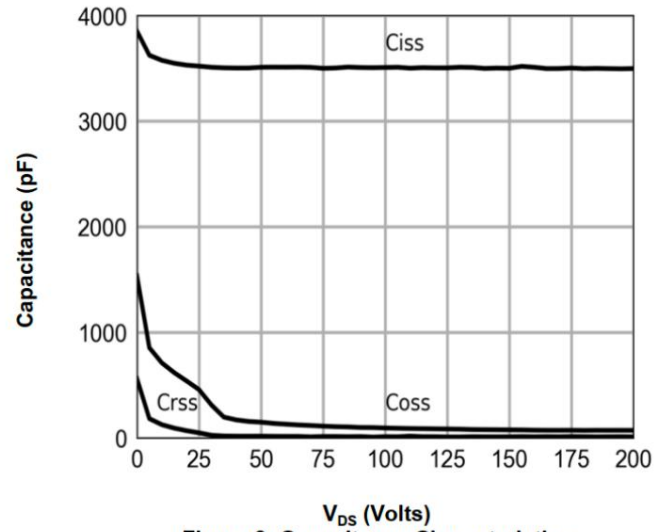


Figure 8: Capacitance Characteristics

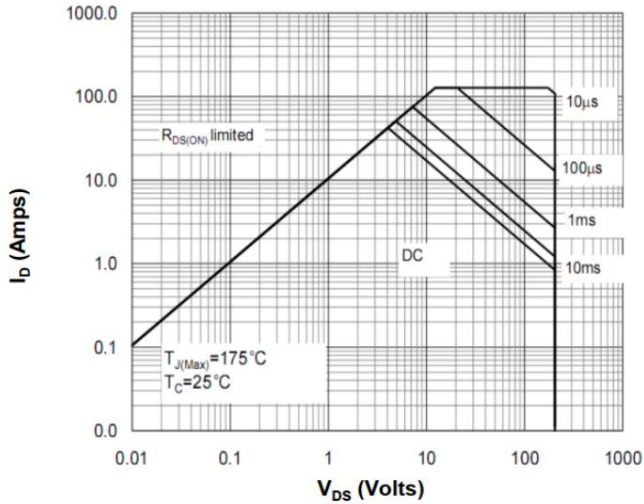


Figure 9: Maximum Forward Biased Safe Operating Area



Test Circuits and Waveforms

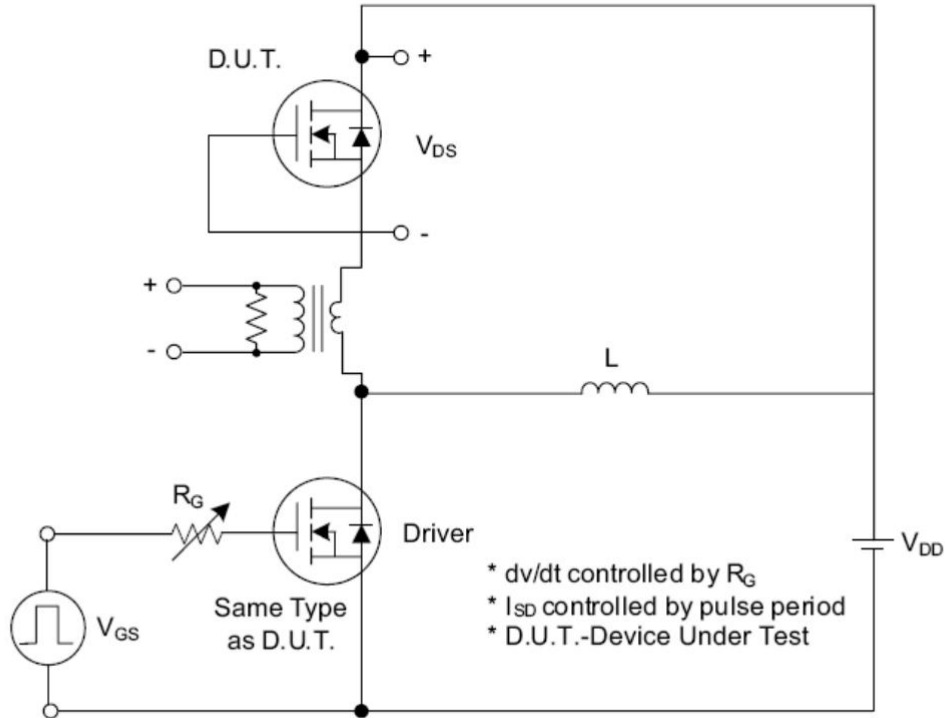


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

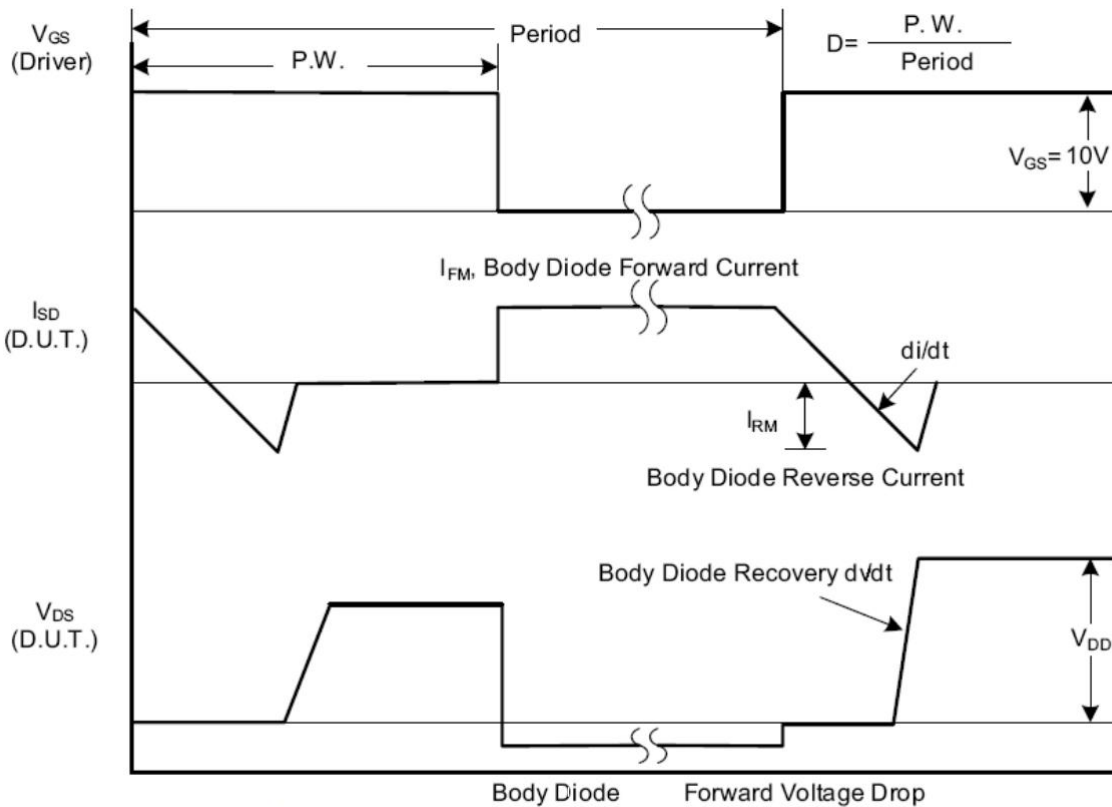


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms



Test Circuits and Waveforms (Cont.)

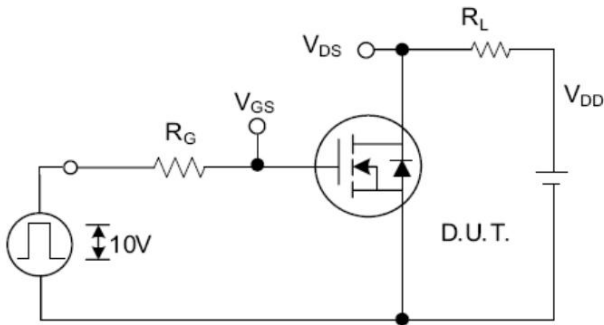


Fig. 2.1 Switching Test Circuit

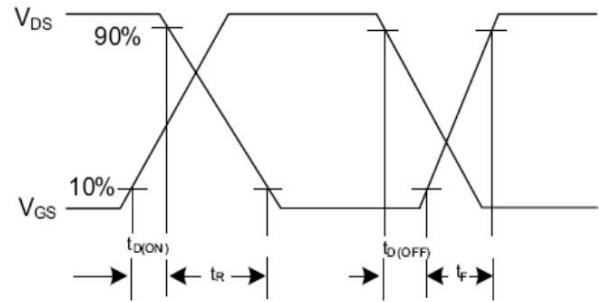


Fig. 2.2 Switching Waveforms

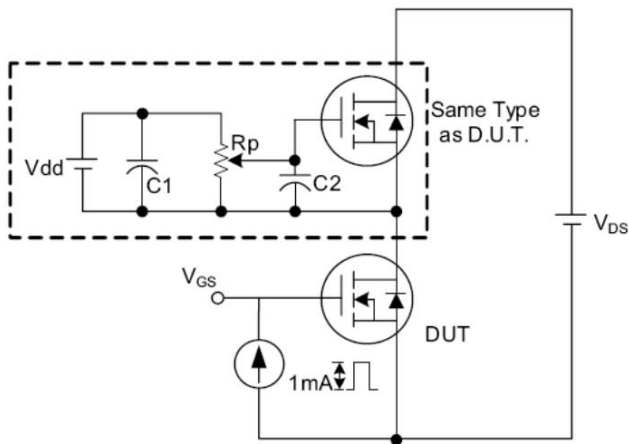


Fig. 3.1 Gate Charge Test Circuit

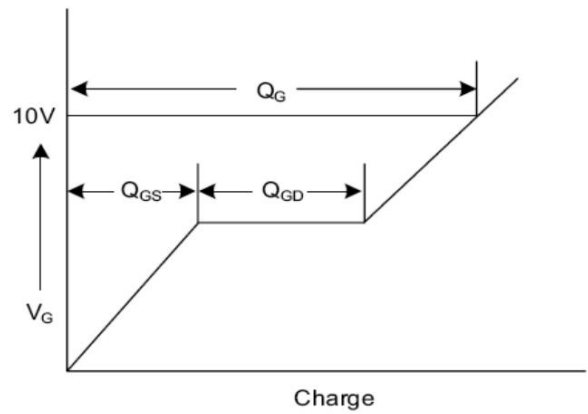


Fig. 3.2 Gate Charge Waveform

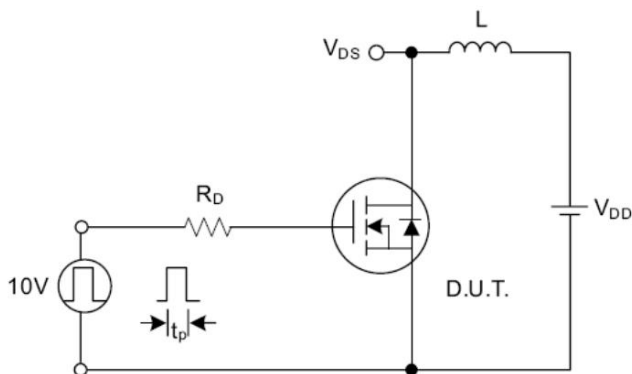


Fig. 4.1 Unclamped Inductive Switching Test Circuit

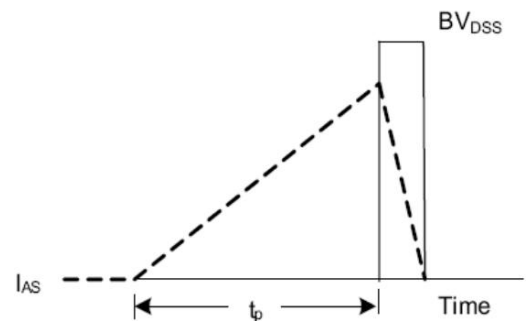
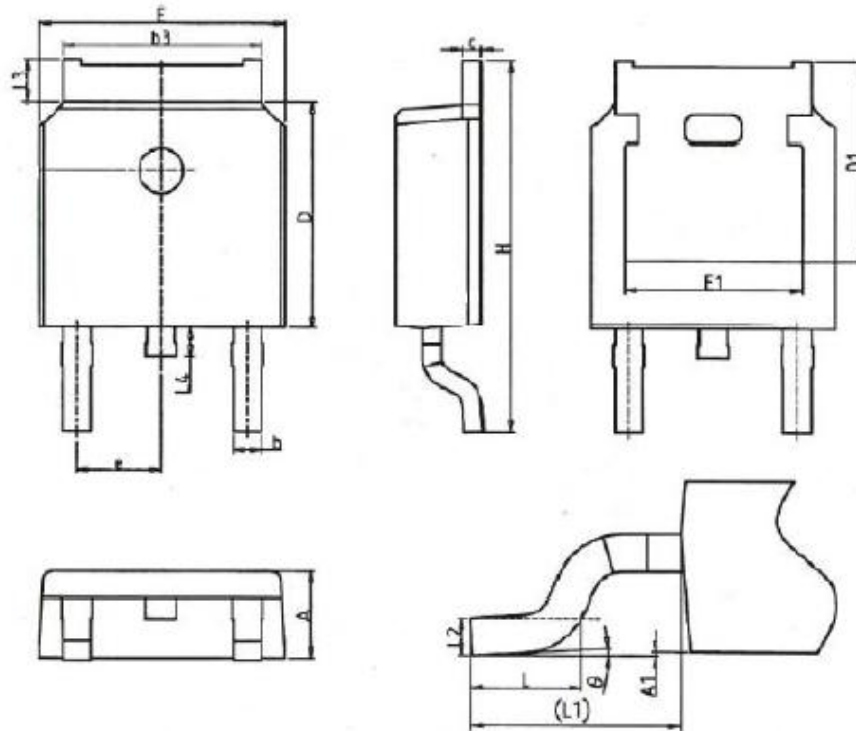


Fig. 4.2 Unclamped Inductive Switching Waveforms



TO252-2L Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.40	0.086	0.095
A1	-	0.2	-	0.008
b	0.68	0.9	0.026	0.036
b3	4.95	5.46	0.194	0.215
c	0.43	0.89	0.017	0.035
D	5.97	6.22	0.235	0.245
D1	5.300REF		0.209REF	
E	6.35	6.73	0.250	0.265
E1	4.32	--	0.170	-
e	2.286BSC		0.09BSC	
H	9.4	10.5	0.370	0.413
L	1.38	1.78	0.054	0.070
L1	2.90REF		0.114REF	
L2	0.51BSC		0.020BSC	
L3	0.88	1.28	0.034	0.050
L4	0.5	1	0.019	0.039
θ	0°	8°	0°	8°