

Description

The HSU60P02 is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

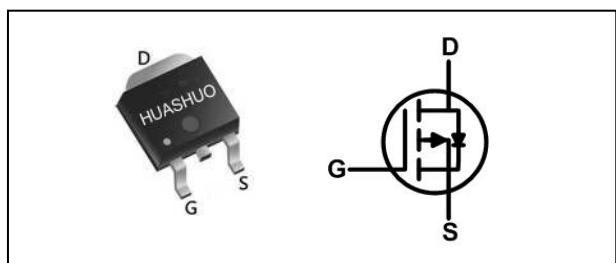
The HSU60P02 meet the RoHS and Green Product requirement with full function reliability approved.

- Super Low Gate Charge
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Product Summary

V _{DS}	-20	V
R _{DSON,typ}	4.1	mΩ
I _D	-60	A

TO-252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	-20	V
V _{GS}	Gate-Source Voltage	± 12	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ -4.5V ¹	-60	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ -4.5V ¹	-39	A
I _{DM}	Pulsed Drain Current ²	-240	A
P _D @T _C =25°C	Total Power Dissipation ³	70	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Max.	Unit
R _{θJC}	Thermal Resistance Junction-Case ¹	2.1	°C/W



Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_{\text{D}}=-250\mu\text{A}$	-20	---	---	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_{\text{D}}=-1\text{mA}$	---	-0.012	---	$\text{V}/^{\circ}\text{C}$
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=-4.5\text{V}$, $I_{\text{D}}=-15\text{A}$	---	4.1	5.5	$\text{m}\Omega$
		$V_{\text{GS}}=-2.5\text{V}$, $I_{\text{D}}=-12\text{A}$	---	6	8.4	
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_{\text{D}}=-250\mu\text{A}$	-0.5	-0.7	-1.0	V
$\Delta V_{\text{GS}(\text{th})}$	$V_{\text{GS}(\text{th})}$ Temperature Coefficient		---	2.94	---	$\text{mV}/^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=-20\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^{\circ}\text{C}$	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 8\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
Q_g	Total Gate Charge (-4.5V)	$V_{\text{DS}}=-10\text{V}$, $V_{\text{GS}}=-4.5\text{V}$, $I_{\text{D}}=-15\text{A}$	---	44	---	nC
Q_{gs}	Gate-Source Charge		---	9.1	---	
Q_{gd}	Gate-Drain Charge		---	11	---	
$T_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{\text{DD}}=-10\text{V}$, $V_{\text{GS}}=-4.5\text{V}$, $R_{\text{G}}=3.3\Omega$, $I_{\text{D}}=-14\text{A}$	---	7	---	ns
T_r	Rise Time		---	61	---	
$T_{\text{d}(\text{off})}$	Turn-Off Delay Time		---	109	---	
T_f	Fall Time		---	44	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=-10\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	4600	---	pF
C_{oss}	Output Capacitance		---	509	---	
C_{rss}	Reverse Transfer Capacitance		---	431	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,4}	$V_G=V_D=0\text{V}$, Force Current	---	---	-60	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	-240	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=-1\text{A}$, $T_J=25^{\circ}\text{C}$	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	$ I_F =-15\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$,	---	24	---	nS
Q_{rr}	Reverse Recovery Charge	$T_J=25^{\circ}\text{C}$	---	11	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_{D} and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Characteristics

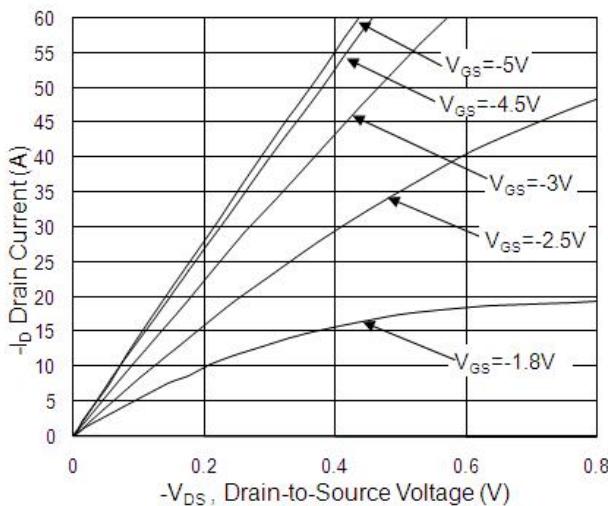


Fig.1 Typical Output Characteristics

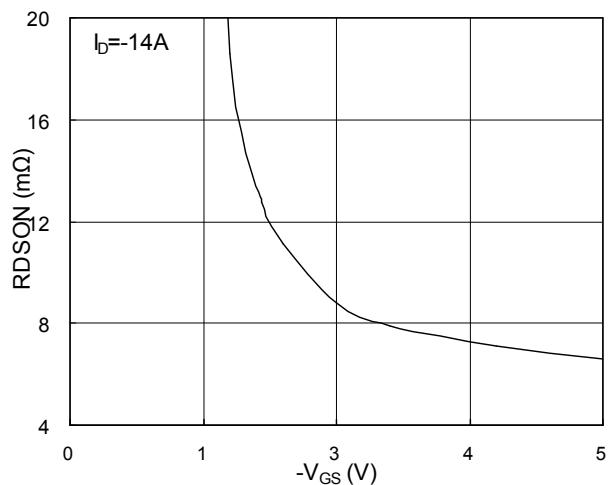


Fig.2 On-Resistance vs. G-S Voltage

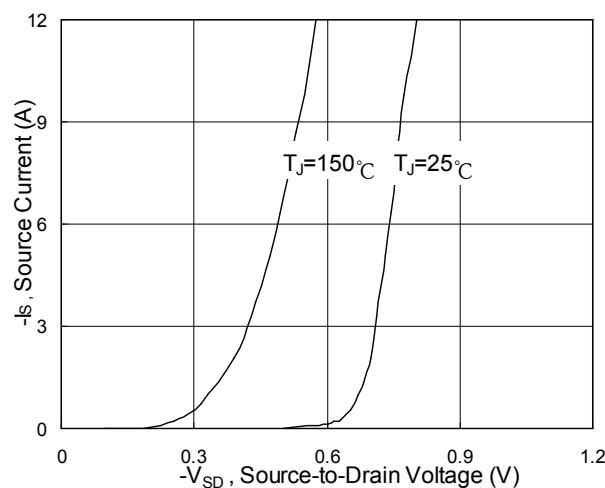


Fig.3 Forward Characteristics of Reverse

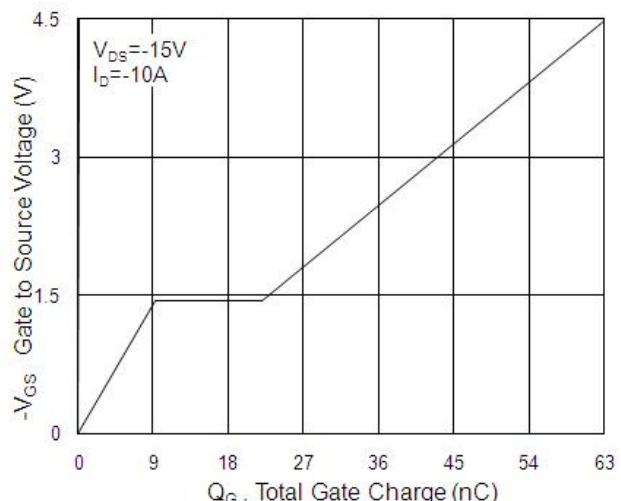


Fig.4 Gate-charge Characteristics

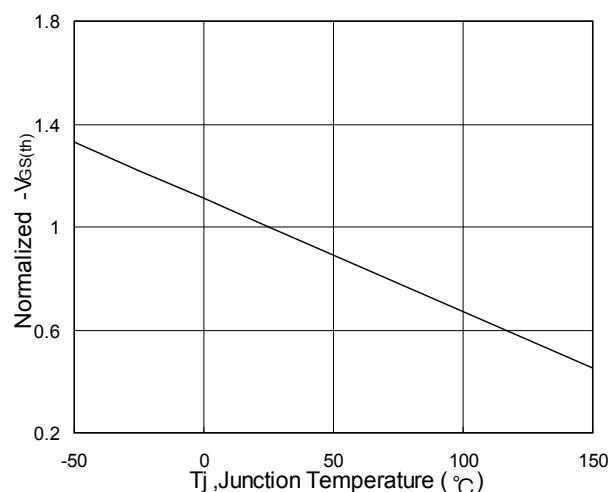


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

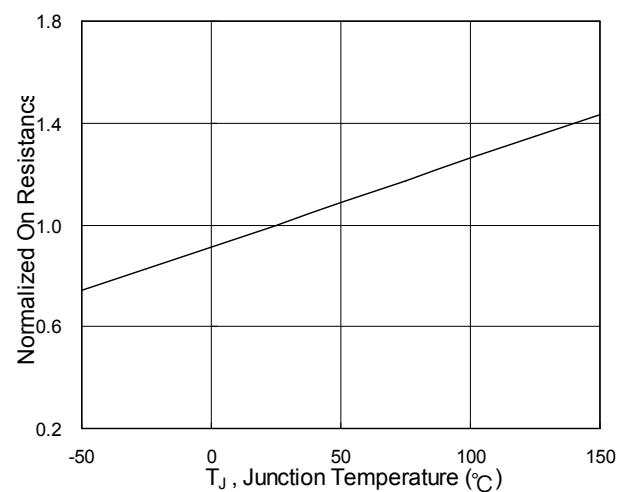


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

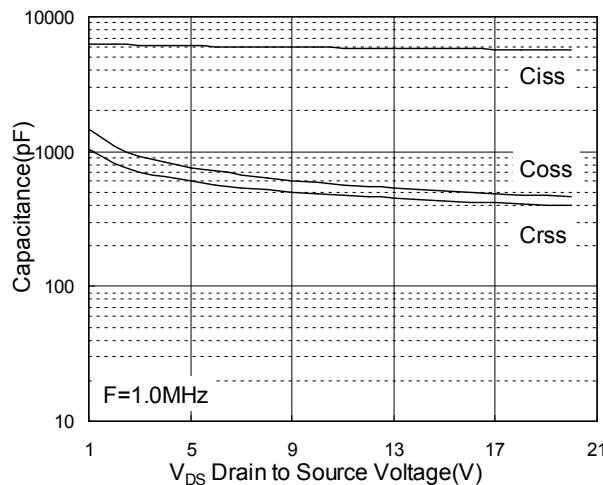


Fig.7 Capacitance

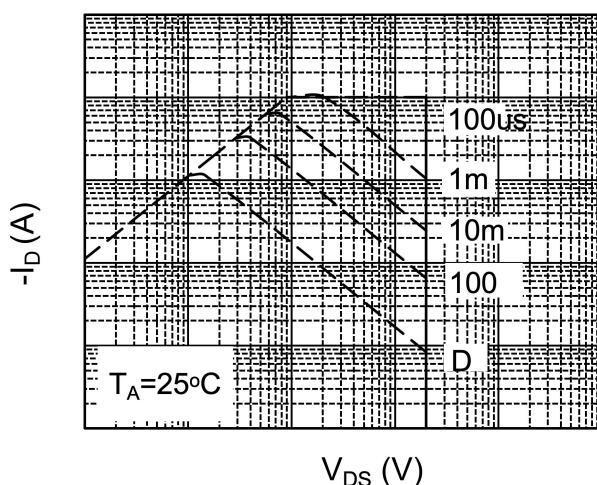


Fig.8 Safe Operating Area

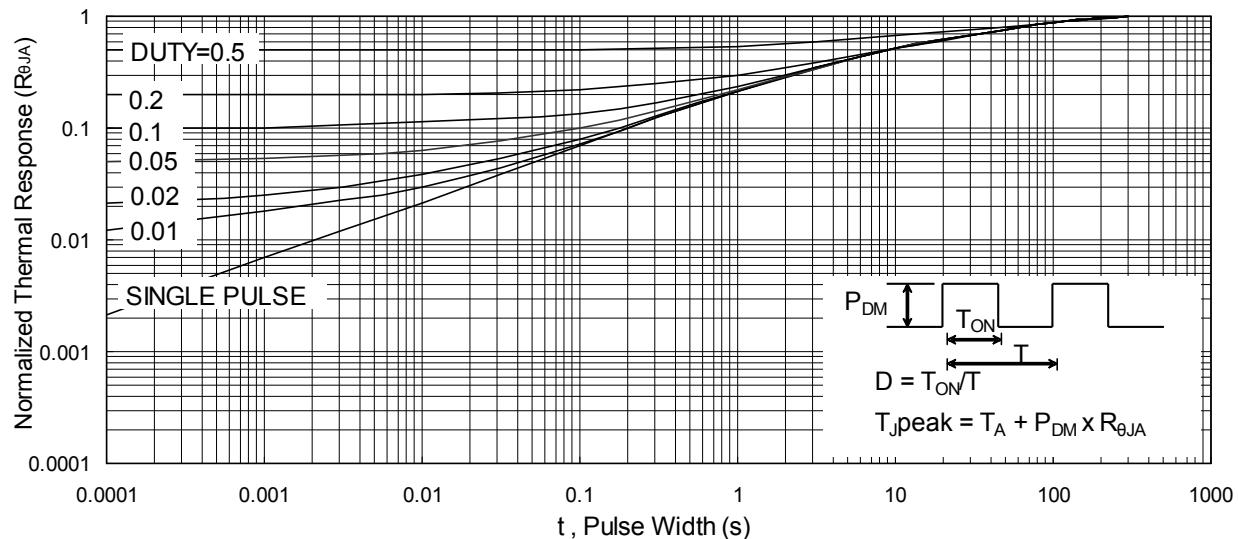


Fig.9 Normalized Maximum Transient Thermal Impedance

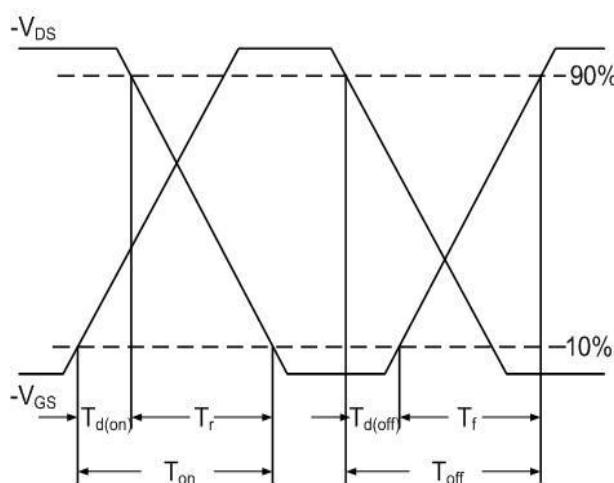


Fig.10 Switching Time Waveform

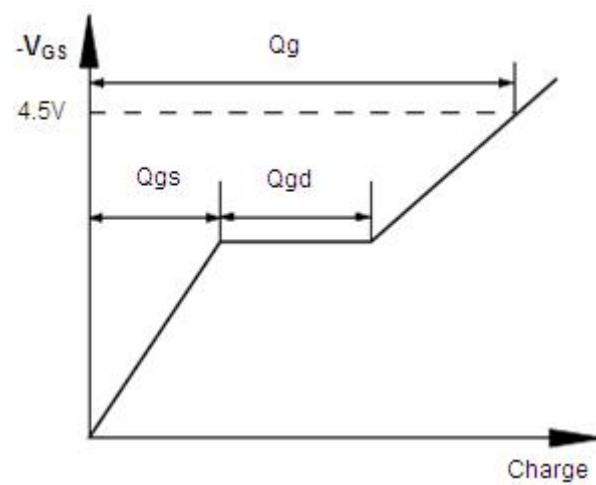
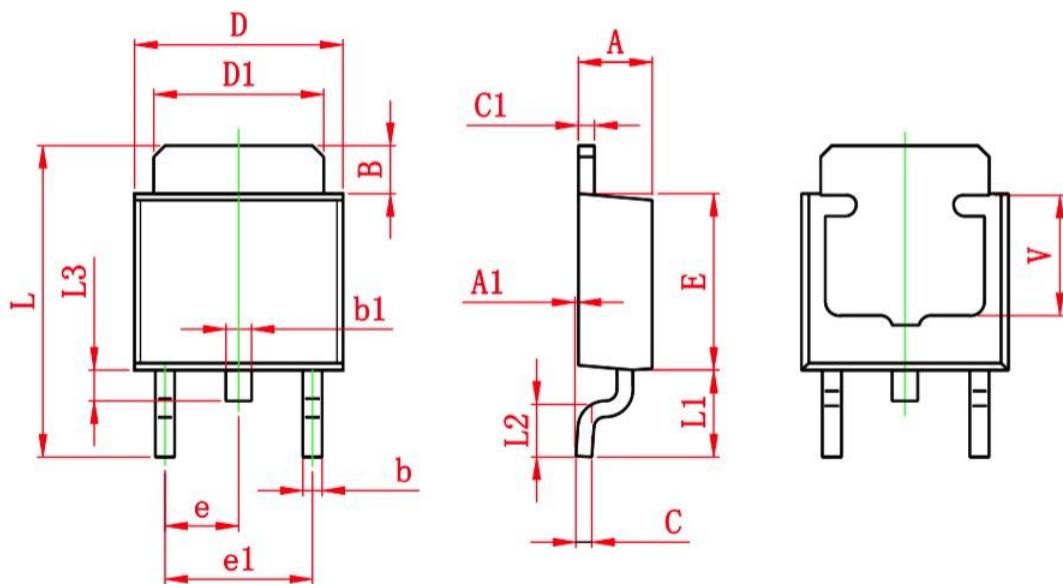


Fig.11 Gate Charge Waveform



Ordering Information

Part Number	Package code	Packaging
HSU60P02	TO-252	2500/Tape&Reel



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	