

**Dual N-Ch 60V Fast Switching MOSFETs**
**Description**

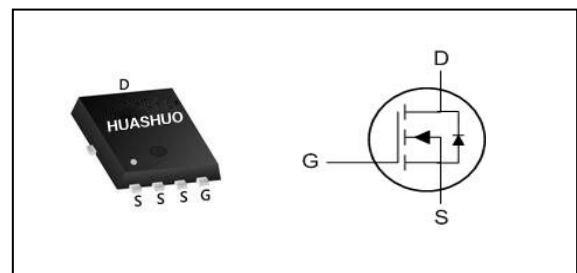
- Advanced Trench MOS Technology
- Low Gate Charge
- Low  $R_{DS(ON)}$
- 100% EAS Guaranteed
- Green Device Available

**Product Summary**

$V_{DS}$	60	V
$R_{DS(ON),typ}$	10	m $\Omega$
$I_D$	50	A

**Application**

- Motor Control.
- DC/DC Converter.
- Synchronous rectifier applications.

**PRPAK5X6 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current <sup>1</sup>	50	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current <sup>1</sup>	35	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	200	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	26.5	mJ
$I_{AS}$	Avalanche Current	15	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	50	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	60	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	2.5	$^\circ\text{C/W}$



**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =15A	---	10	12	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A	---	14	16	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	---	2.3	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> = ± 20V, V <sub>DS</sub> =0V	---	---	± 100	nA
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	1.3	---	Ω
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =30V, V <sub>GS</sub> =10V, I <sub>D</sub> =15A	---	15	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	3.5	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	4.2	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =15A	---	7	---	ns
T <sub>r</sub>	Rise Time		---	4.5	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	26	---	
T <sub>f</sub>	Fall Time		---	5	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1MHz	---	1270	---	pF
C <sub>oss</sub>	Output Capacitance		---	478	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	40	---	

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	50	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>		---	---	200	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =A, T <sub>J</sub> =25°C	---	---	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> =15A, dI/dt=100A/μs,	---	22	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge	T <sub>J</sub> =25°C	---	72	---	nC

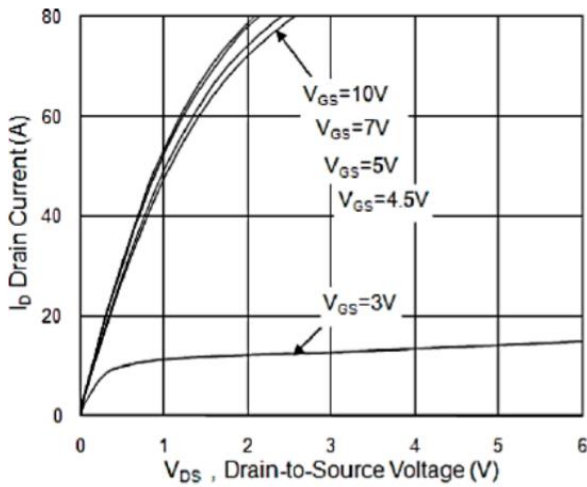
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=15A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

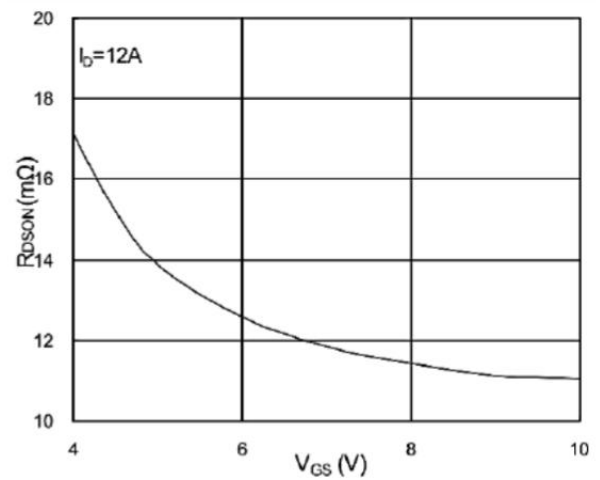


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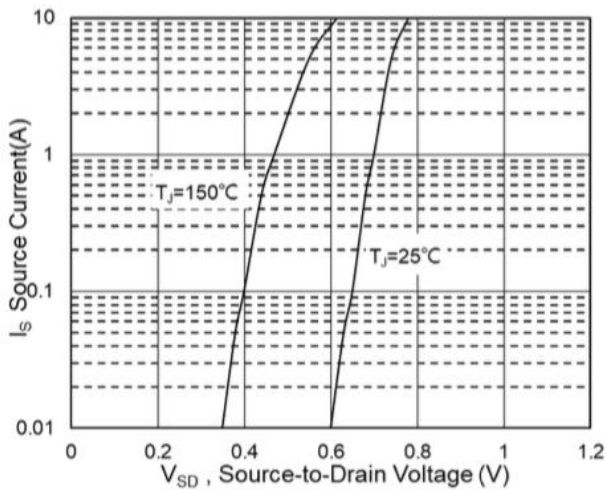
**Typical Characteristics**



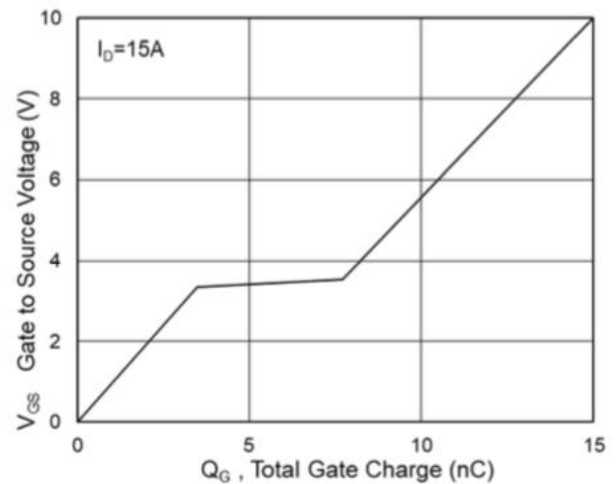
**Fig.1 Typical Output Characteristics**



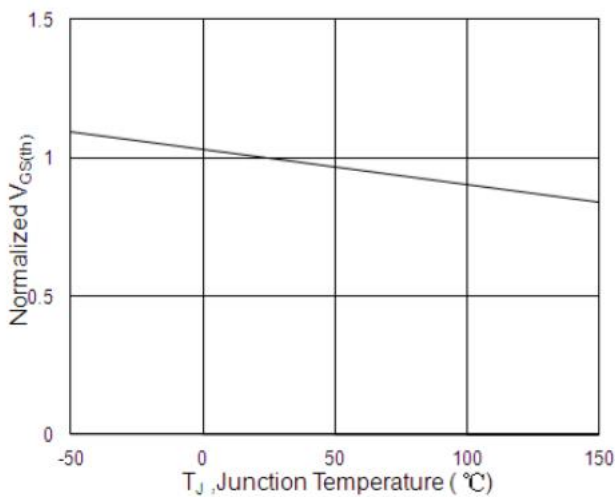
**Fig.2 On-Resistance vs. Gate-Source Voltage**



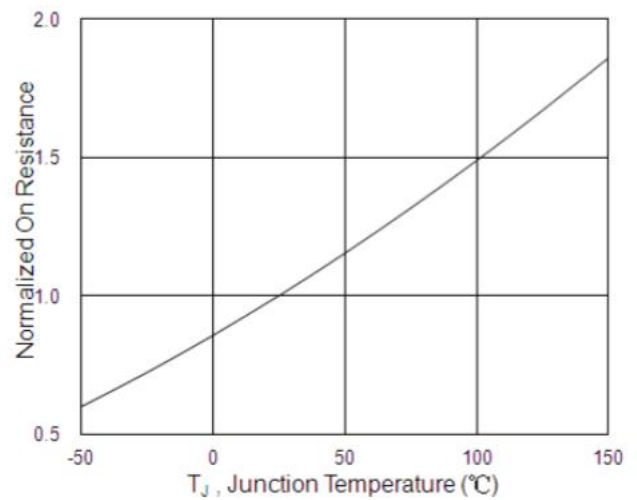
**Fig.3 Source Drain Forward Characteristics**



**Fig.4 Gate-Charge Characteristics**



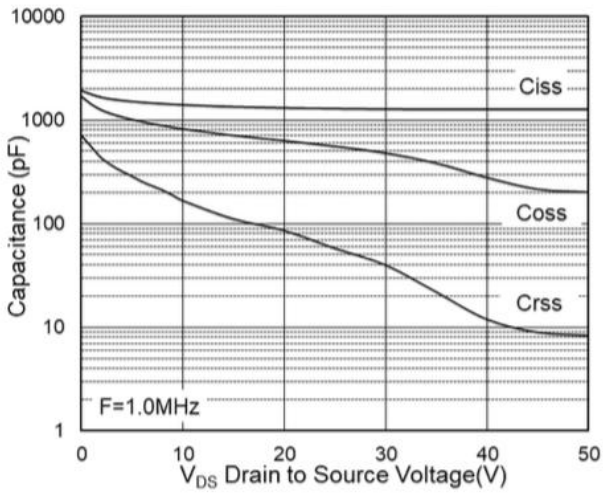
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



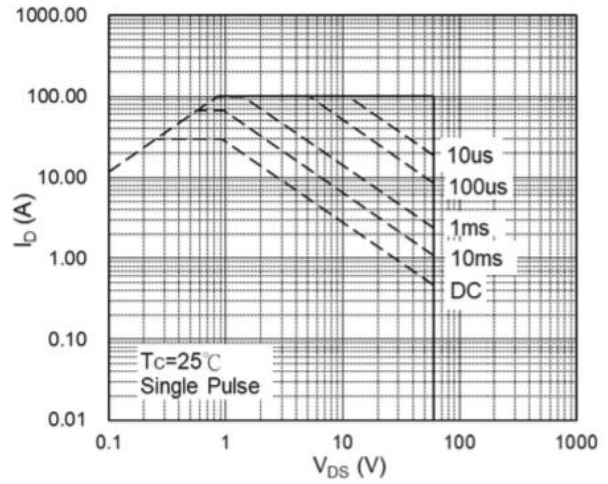
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



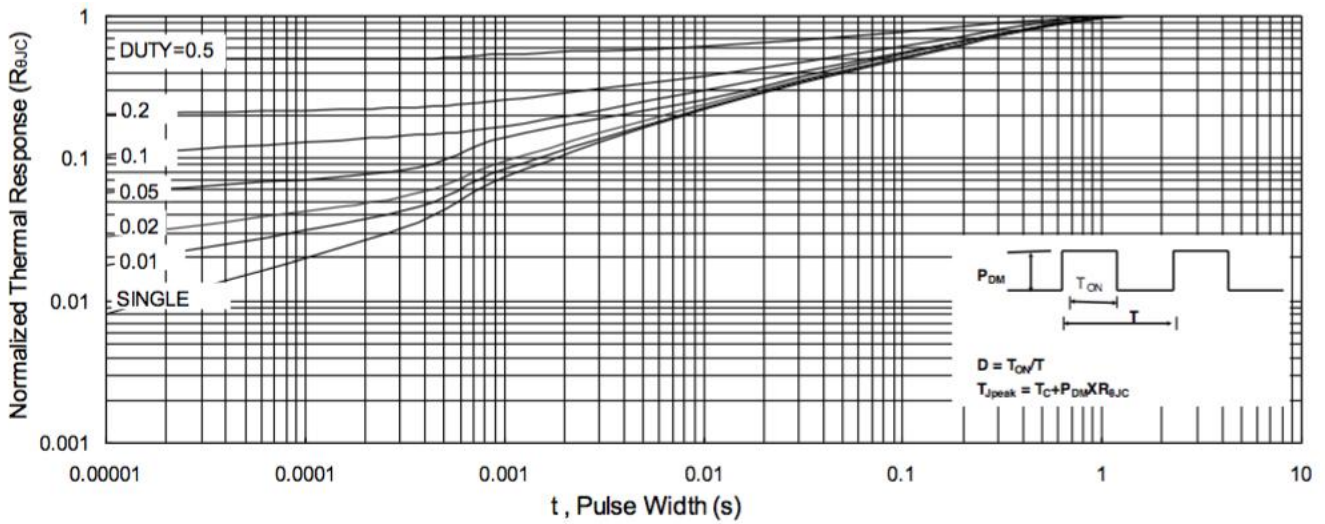
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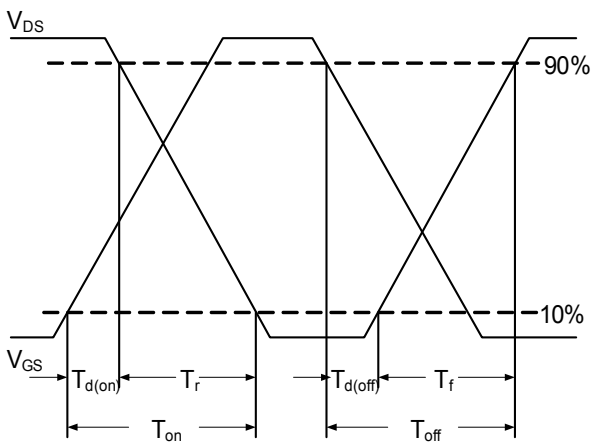
**Fig.7 Capacitance**



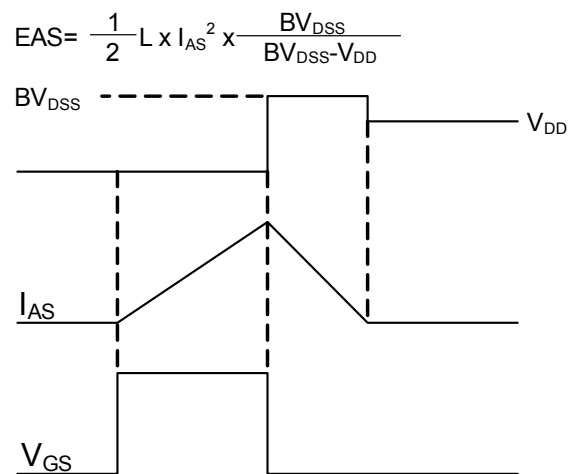
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



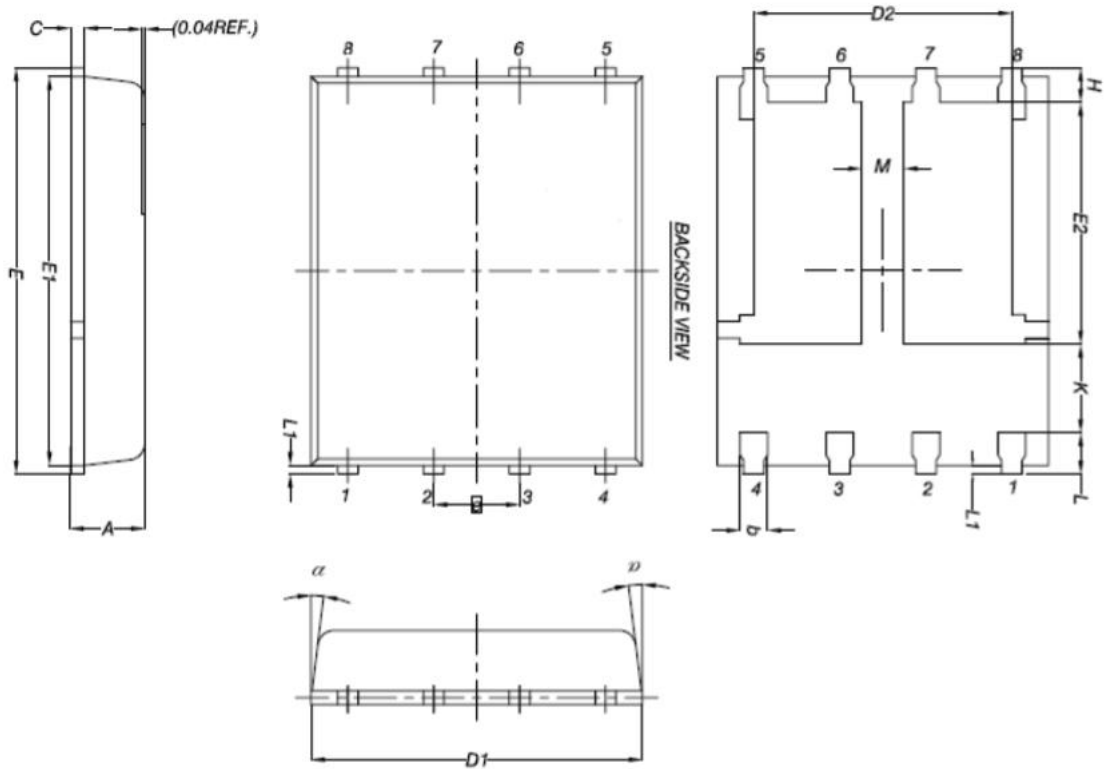
**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**



## PRPAK5x6-8L Dual EP2 Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.17	0.035	0.046
b	0.33	0.51	0.013	0.020
C	0.20	0.30	0.008	0.012
D1	4.80	5.20	0.189	0.205
D2	3.61	3.96	0.142	0.156
E	5.90	6.15	0.232	0.242
E1	5.70	5.85	0.224	0.230
E2	3.30	3.78	0.130	0.149
e	1.27 BSC		0.05 BSC	
H	0.38	0.61	0.015	0.024
K	1.10	---	0.043	---
L	0.38	0.61	0.015	0.024
L1	0.05	0.25	0.002	0.010
M	0.50	---	0.020	---
α	0°	12°	0°	12°