



## Description

The HSU6048 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

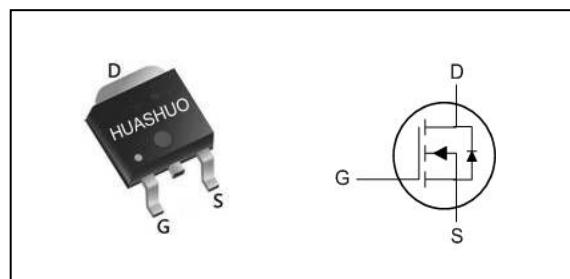
The HSU6048 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

## Product Summary

V <sub>DS</sub>	60	V
R <sub>DSON(TYP)</sub>	3.5	mΩ
I <sub>D</sub>	90	A

- Super Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

## TO-252 Pin Configuration



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	60	V
V <sub>GS</sub>	Gate-Source Voltage	± 20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current <sup>1,6</sup>	90	A
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current <sup>1,6</sup>	67	A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	240	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	101	mJ
I <sub>AS</sub>	Avalanche Current	54	A
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	60	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

## Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance Junction-Ambient <sup>1</sup>	---	60	°C/W
R <sub>θJC</sub>	Thermal Resistance Junction-Case <sup>1</sup>	---	1.8	°C/W



**N-Ch 60V Fast Switching MOSFETs**

**Electrical Characteristics ( $T_J=25$  °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=20A$	---	3.5	3.6	$m\Omega$
		$V_{GS}=4.5V, I_D=15A$	---	4.7	5.4	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.3	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=48V, V_{GS}=0V, T_J=25^\circ C$	---	---	1	$\mu A$
		$V_{DS}=48V, V_{GS}=0V, T_J=55^\circ C$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V, I_D=20A$	---	65	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	0.7	---	$\Omega$
$Q_g$	Total Gate Charge (10V)	$V_{DS}=30V, V_{GS}=10V, I_D=20A$	---	58	---	nC
$Q_{gs}$	Gate-Source Charge		---	16	---	
$Q_{gd}$	Gate-Drain Charge		---	4	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V, V_{GS}=10V, R_G=3\Omega, I_D=20A$	---	18	---	ns
$T_r$	Rise Time		---	8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	50	---	
$T_f$	Fall Time		---	10.5	---	
$C_{iss}$	Input Capacitance	$V_{DS}=30V, V_{GS}=0V, f=1MHz$	---	3458	---	pF
$C_{oss}$	Output Capacitance		---	1522	---	
$C_{rss}$	Reverse Transfer Capacitance		---	22	---	

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_s$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V$ , Force Current	---	---	90	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_s=1A, T_J=25^\circ C$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=20A, dI/dt=100A/\mu s, T_J=25^\circ C$	---	24	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	85	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=50V, V_{GS}=10V, L=0.1mH, I_{AS}=54A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.
- 6.The maximum current rating is package limited.



### Typical Characteristics

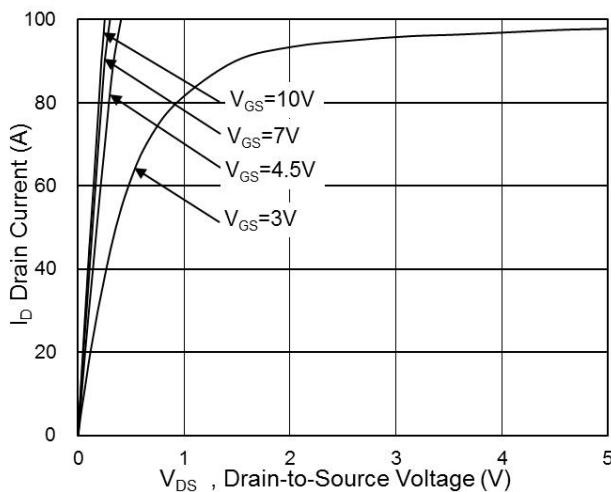


Fig.1 Typical Output Characteristics

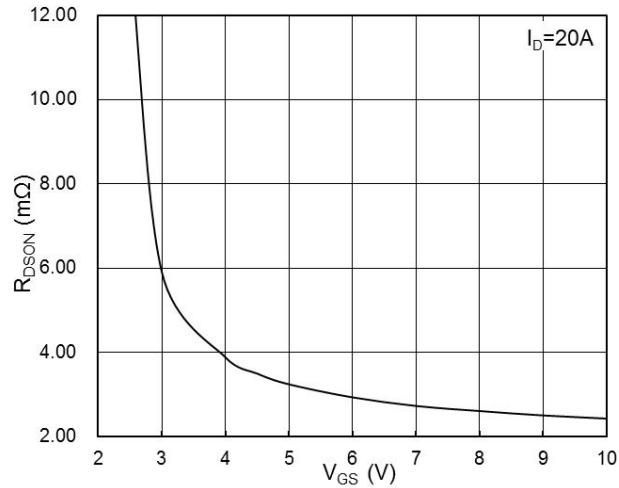


Fig.2 On-Resistance vs G-S Voltage

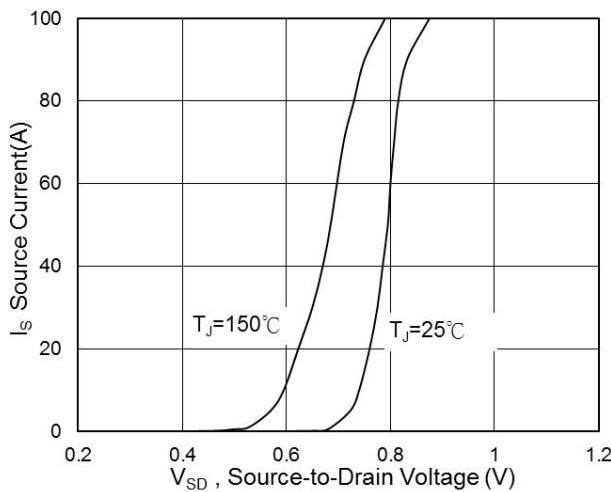


Fig.3 Diode Forward Voltage vs. Current

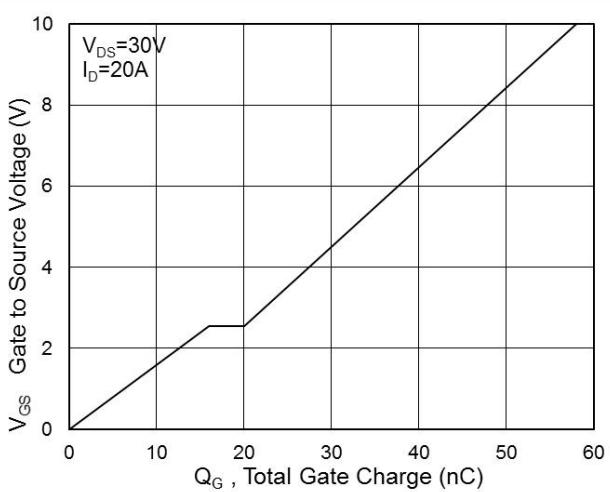


Fig.4 Gate-Charge Characteristics

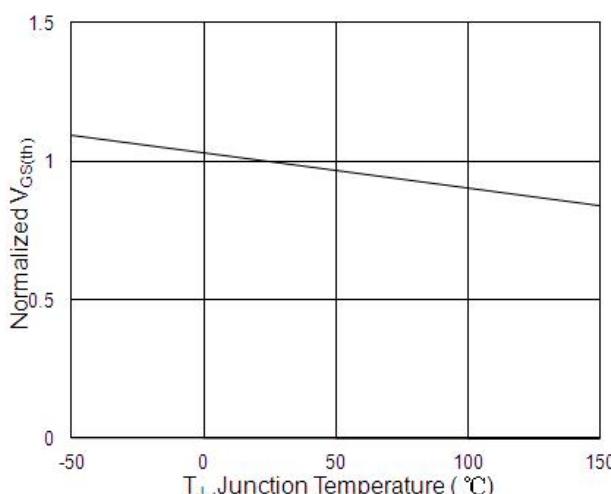


Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$

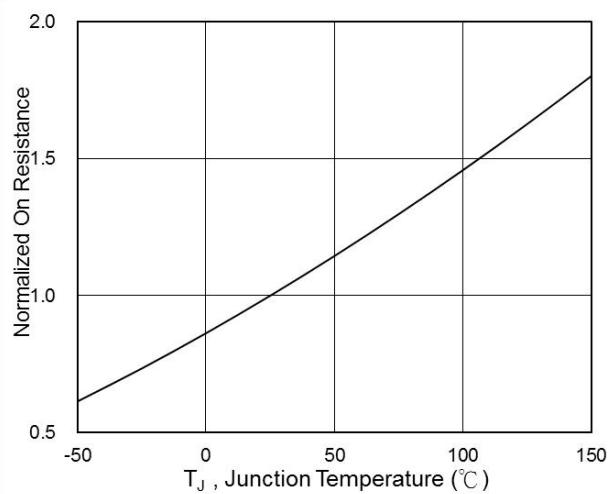


Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$



N-Ch 60V Fast Switching MOSFETs

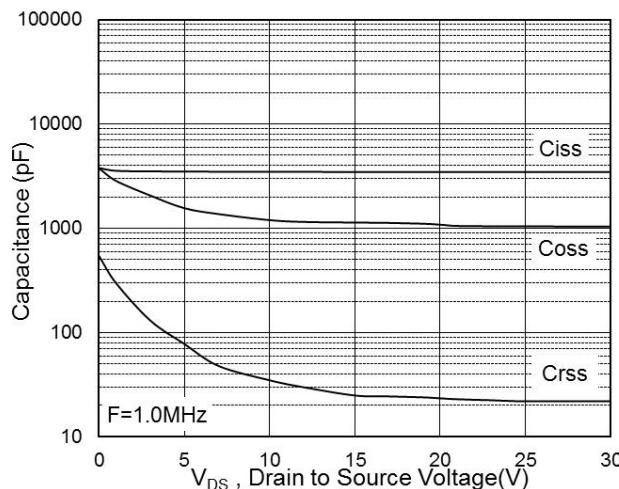


Fig.7 Capacitance

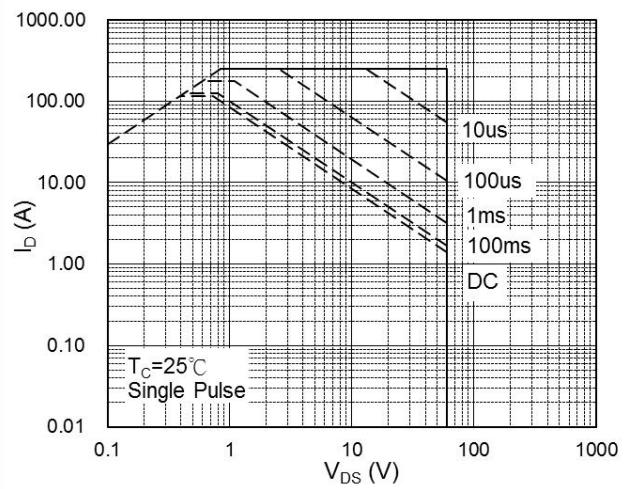


Fig.8 Safe Operating Area

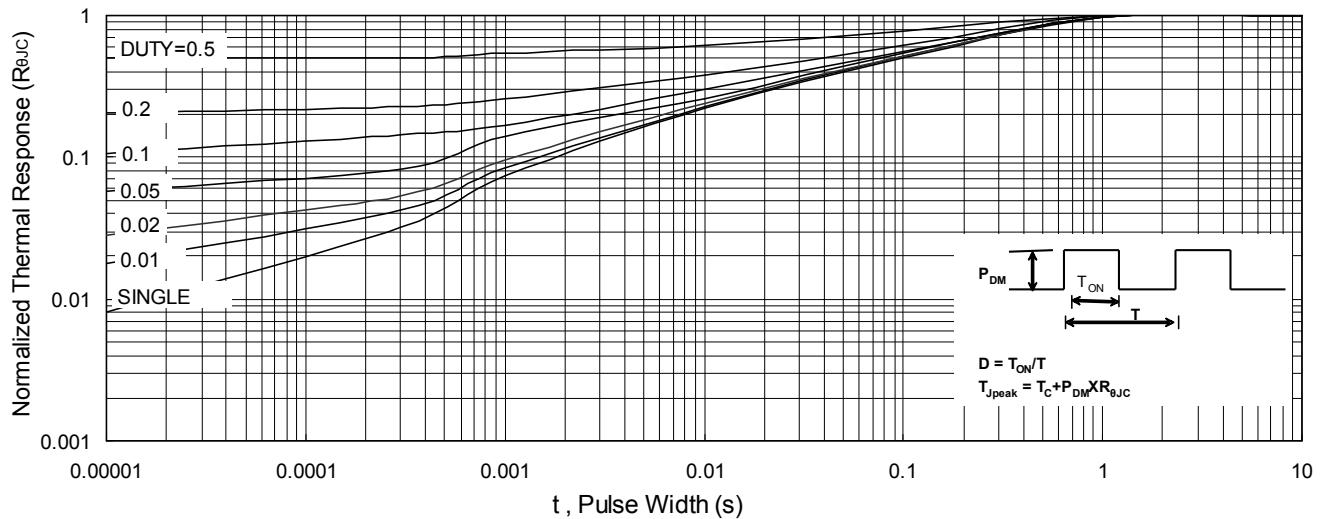


Fig.9 Normalized Maximum Transient Thermal Impedance

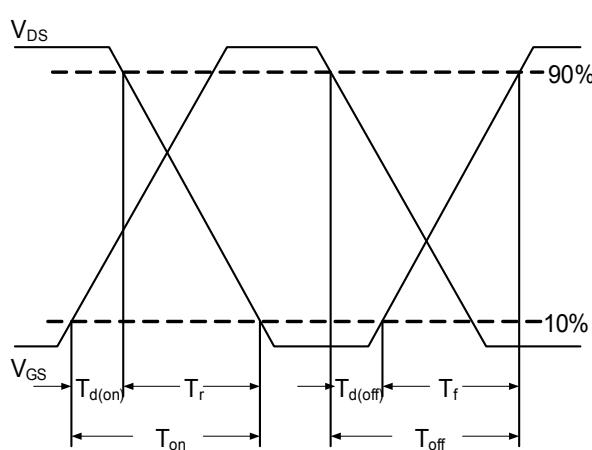


Fig.10 Switching Time Waveform

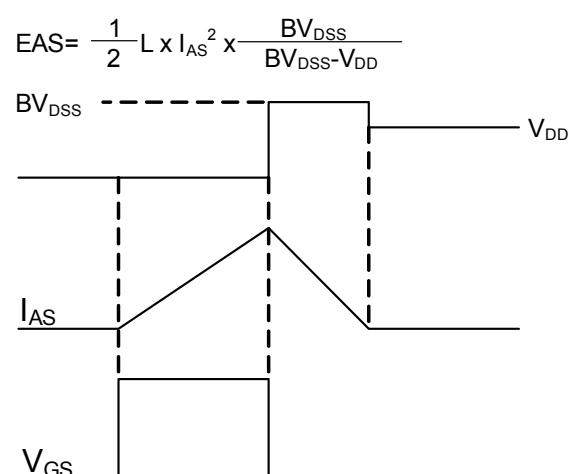
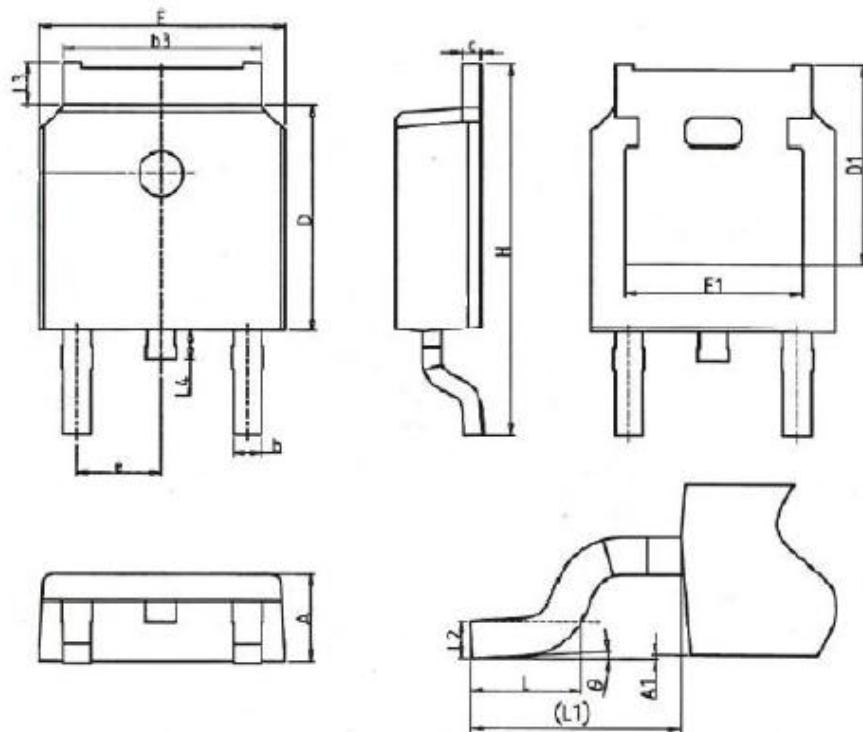


Fig.11 Unclamped Inductive Switching



## TO252-2L Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.40	0.086	0.095
A1	-	0.2	-	0.008
b	0.68	0.9	0.026	0.036
b3	4.95	5.46	0.194	0.215
c	0.43	0.89	0.017	0.035
D	5.97	6.22	0.235	0.245
D1	5.300REF		0.209REF	
E	6.35	6.73	0.250	0.265
E1	4.32	--	0.170	-
e	2.286BSC		0.09BSC	
H	9.4	10.5	0.370	0.413
L	1.38	1.78	0.054	0.070
L1	2.90REF		0.114REF	
L2	0.51BSC		0.020BSC	
L3	0.88	1.28	0.034	0.050
L4	0.5	1	0.019	0.039
Θ	0°	8°	0°	8°