

**Description**

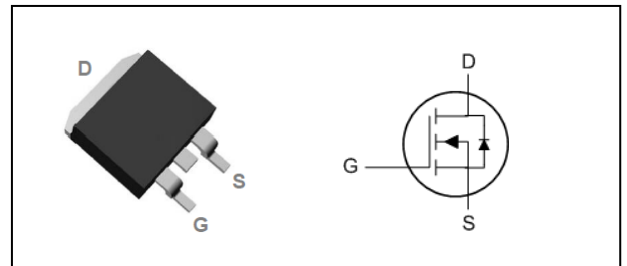
The HSH8004 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The HSH8004 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

**Product Summary**

$V_{DS}$	80	V
$R_{DS(ON),TYP}$	3.1	m $\Omega$
$I_D$	175	A

**TO-263 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	80	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	175	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	123	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	440	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	378	mJ
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	192	W
$T_{STG}$	Storage Temperature Range	-55 to 175	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 175	$^\circ C$

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	0.65	$^\circ C/W$



**Electrical Characteristics ( $T_J=25\text{ }^\circ\text{C}$ , unless otherwise noted)**

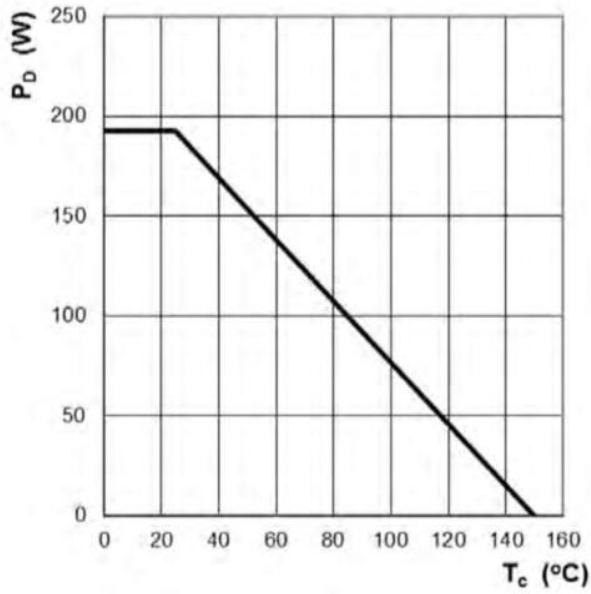
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	80	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=20A$	---	3.1	3.5	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.8	2.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{DS}=64V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	100	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	50	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.2	---	$\Omega$
$Q_g$	Total Gate Charge (10V)	$V_{DD}=40V, V_{GS}=10V, I_D=20A$	---	80	---	nC
$Q_{gs}$	Gate-Source Charge		---	15	---	
$Q_{gd}$	Gate-Drain Charge		---	16	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=40V, V_{GS}=10V, R_G=6\Omega, I_D=20A$	---	17	---	ns
$T_r$	Rise Time		---	32	---	
$T_{d(off)}$	Turn-Off Delay Time		---	50	---	
$T_f$	Fall Time		---	18	---	
$C_{iss}$	Input Capacitance	$V_{DS}=40V, V_{GS}=0V, f=1\text{MHz}$	---	4450	---	pF
$C_{oss}$	Output Capacitance		---	800	---	
$C_{rss}$	Reverse Transfer Capacitance		---	50	---	

**Diode Characteristics**

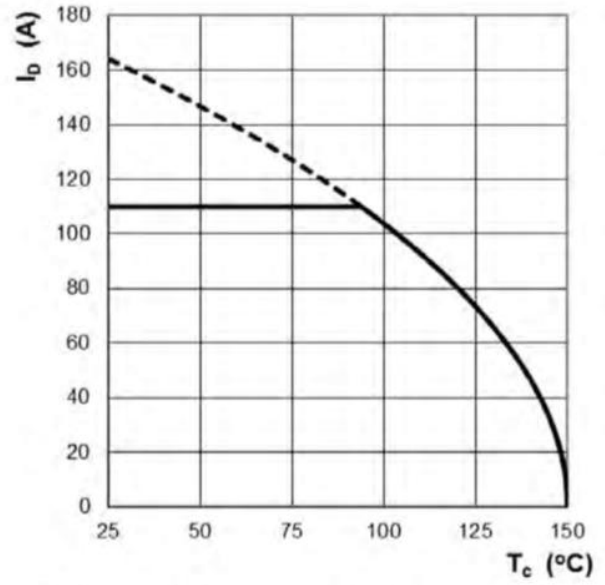
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	175	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=A, T_J=25^\circ\text{C}$	---	---	1.5	V
$t_{rr}$	Reverse Recovery Time	$I_F=20A, dI/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	40	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	45	---	nC



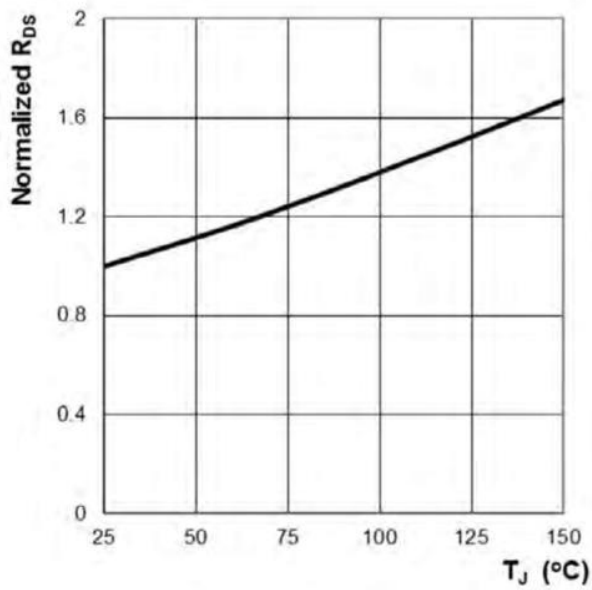
**Electrical Characteristic Diagrams**



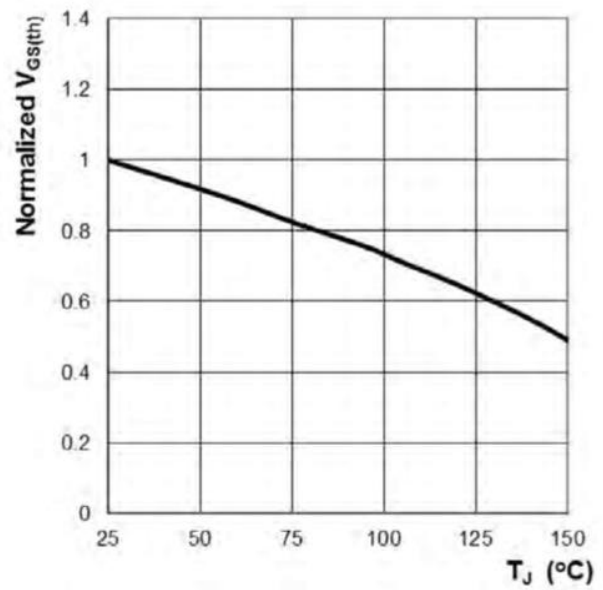
**Figure 1: Power Dissipation**



**Figure 2: Continuous Drain Current vs.  $T_c$**



**Figure 3: Normalized  $R_{DS(ON)}$  vs.  $T_J$**



**Figure 4: Normalized  $BV_{DSS}$  vs.  $T_J$**

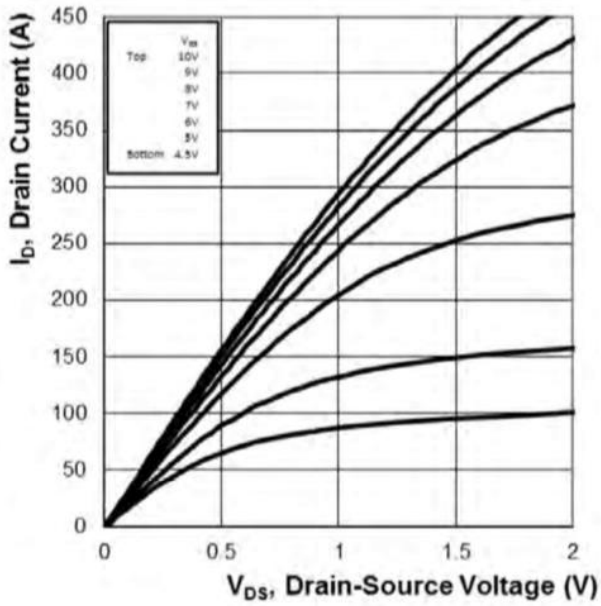


Figure 5: On-Region Characteristics

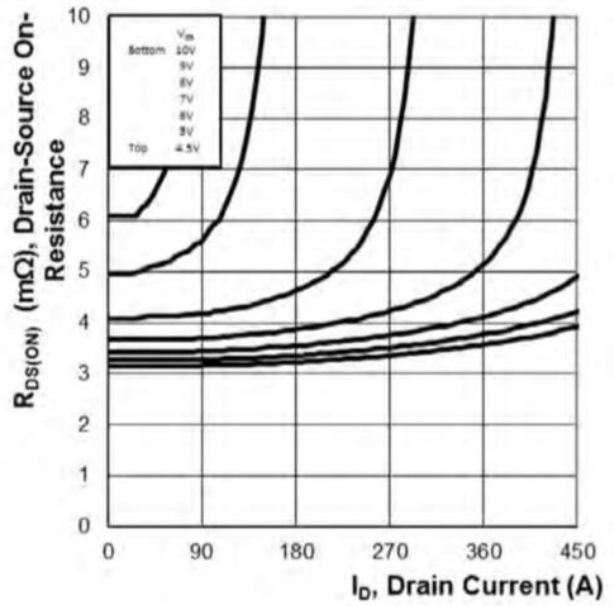


Figure 6: Typ.  $R_{DS}$  Variation vs.  $I_D$  and  $V_{GS}$

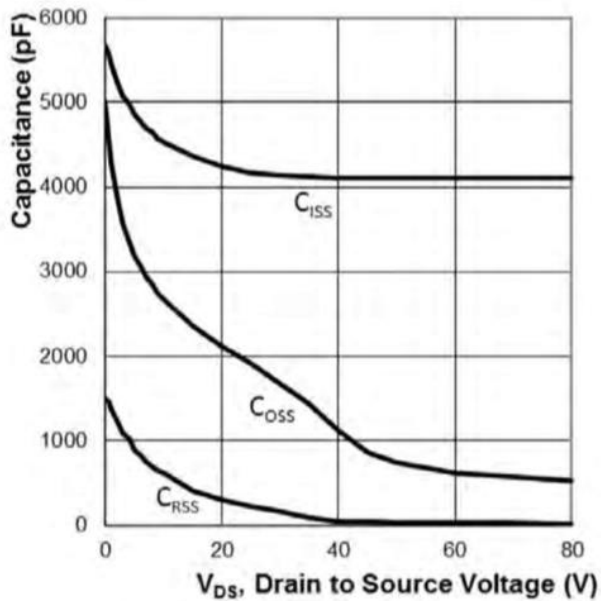


Figure 7: Typ. Capacitance Characteristics

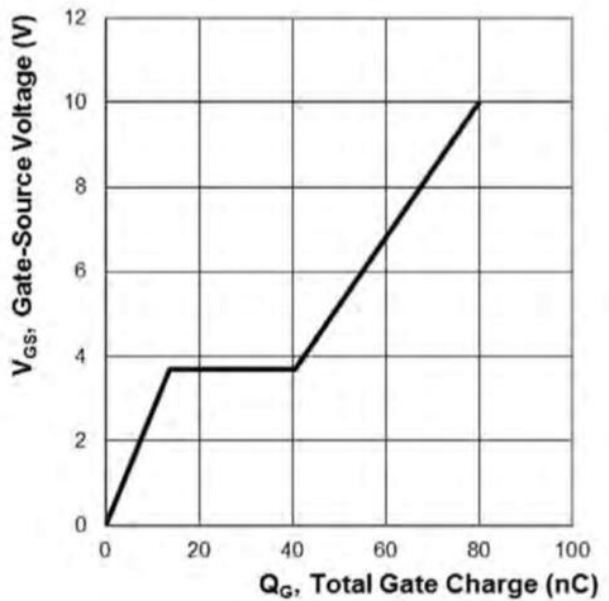


Figure 8: Typ. Gate Charge Characteristics

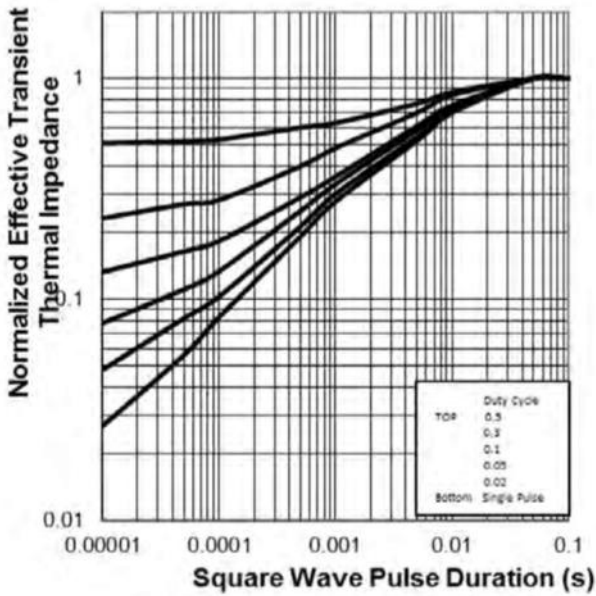


Figure 9: Normalized Thermal Transient Impedance, Junction-to-Case

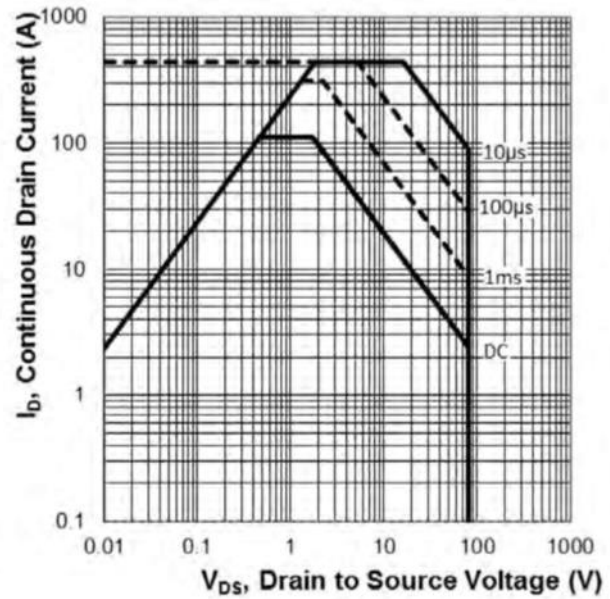


Figure 10: Maximum Safe Operation Area

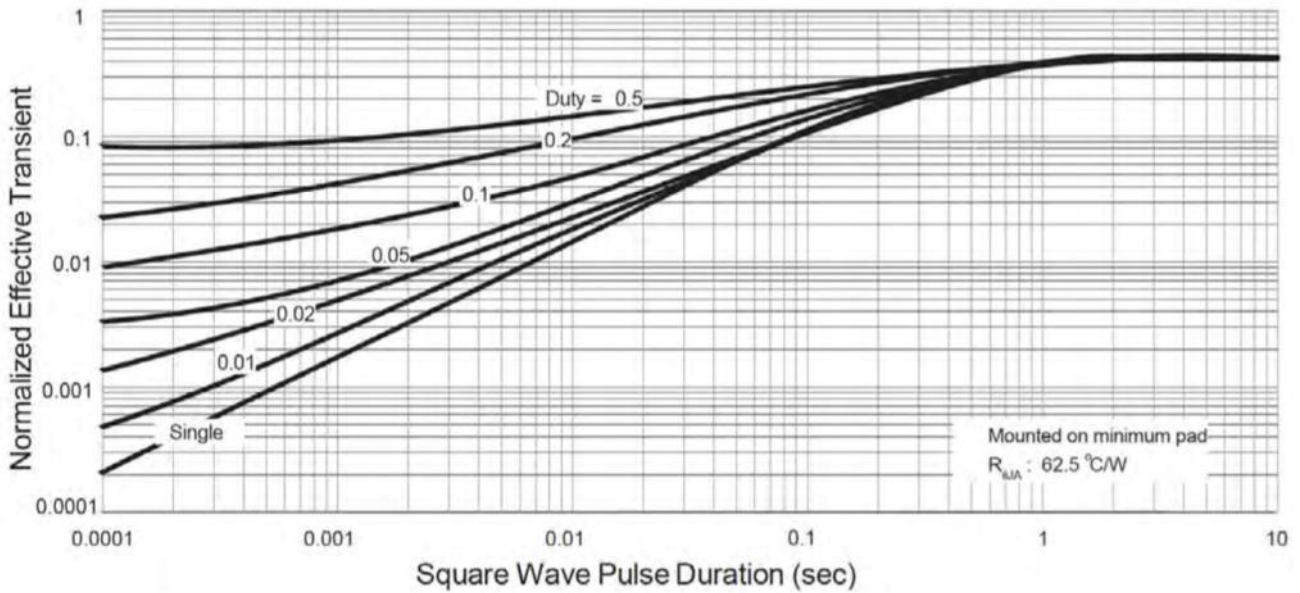


Fig 7 Normalized Maximum Transient Thermal Impedance



Parameter Test Circuits

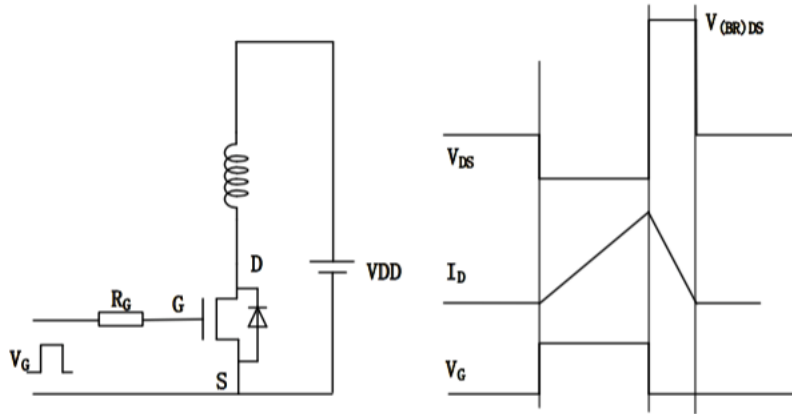


Figure 10 Unclamped Inductive Switching (UIS) Test circuit and waveforms

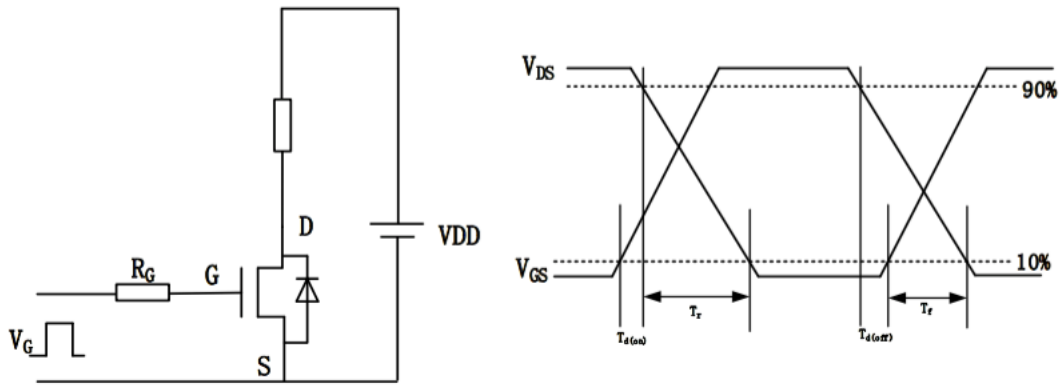


Figure 11 Resistive Switching time Test circuit and waveforms

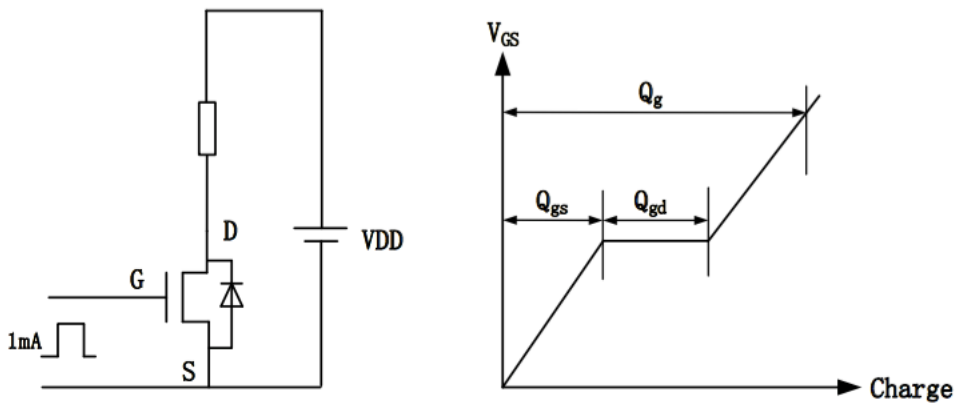


Figure 12 Gate charge Test circuit and waveforms