

Description

The HSM4606 is the high performance complementary N-ch and P-ch MOSFETs with high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

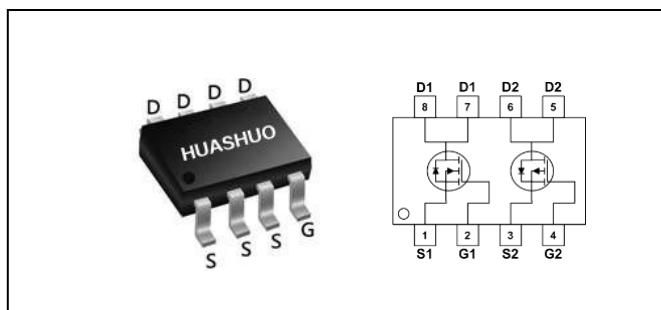
The HSM4606 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Product Summary

BVDSS	RDSON	ID
30V	22mΩ	7A
-30V	26mΩ	-6A

SOP8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V _{DS}	Drain-Source Voltage	30	-30	V
V _{GS}	Gate-Source Voltage	±20	±20	V
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ₁	7	-6	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ₁	4.8	-4.5	A
I _{DM}	Pulsed Drain Current ²	24	-24	A
EAS	Single Pulse Avalanche Energy ³	8.1	45	mJ
I _{AS}	Avalanche Current	12.7	-30	A
P _D @T _A =25°C	Total Power Dissipation ⁴	1.5	1.5	W
T _{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	85	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	60	°C/W

N-Channel Electrical Characteristics ($T_J=25^\circ C$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to $25^\circ C, I_D=1mA$	---	0.023	---	$^\circ C$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=6A$	---	22	28	$m\Omega$
		$V_{GS}=4.5V, I_D=4A$	---	35	41	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	---	3	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.2	---	$mV/^\circ C$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ C$	---	---	1	μA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ C$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=6A$	---	12.8	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	2.3	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=20V, V_{GS}=4.5V, I_D=6A$	---	7	---	nC
Q_{gs}	Gate-Source Charge		---	1.6	---	
Q_{gd}	Gate-Drain Charge		---	1.6	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=12V, V_{GS}=10V, R_G=3.3\Omega$ $I_D=6A$	---	7.7	---	ns
T_r	Rise Time		---	46	---	
$T_{d(off)}$	Turn-Off Delay Time		---	11	---	
T_f	Fall Time		---	3.6	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	388	---	pF
C_{oss}	Output Capacitance		---	62	---	
C_{rss}	Reverse Transfer Capacitance		---	58	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	6	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	24	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_s=1A, T_J=25^\circ C$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=12.7A$
- 4.The power dissipation is limited by $150^\circ C$ junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-30	---	---	V
△BV _{DSS} /△T _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.021	---	V/°C
R _{DSON}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-6A	---	26	32	mΩ
		V _{GS} =-4.5V, I _D =-4A	---	35	56	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250μA	-1.0	---	-3.0	V
△V _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-4.2	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-6A	---	12.6	---	S
R _G	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	15	---	---	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-20V, V _{GS} =-4.5V, I _D =-6A	---	18.6	---	nC
Q _{gs}	Gate-Source Charge		---	3.5	---	
Q _{gd}	Gate-Drain Charge		---	2.3	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-24V, V _{GS} =-10V, R _G =3.3Ω, I _D =-1A	---	16.4	---	ns
T _r	Rise Time		---	20.2	---	
T _{d(off)}	Turn-Off Delay Time		---	55	---	
T _f	Fall Time		---	10	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	926	---	pF
C _{oss}	Output Capacitance		---	119	---	
C _{rss}	Reverse Transfer Capacitance		---	97	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-5.7	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	-24	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-30A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



N-Channel Typical Characteristics

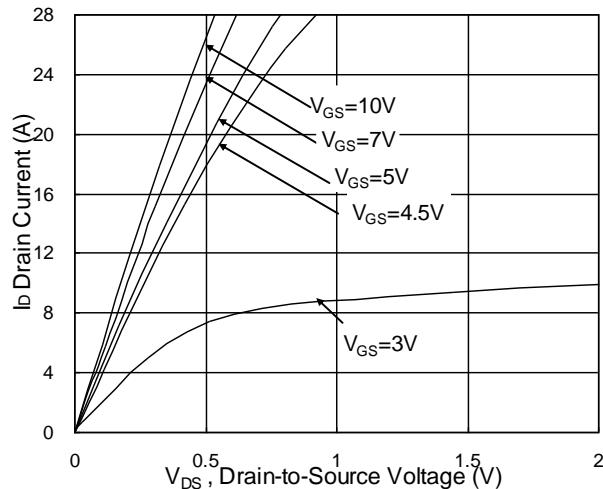


Fig.1 Typical Output Characteristics

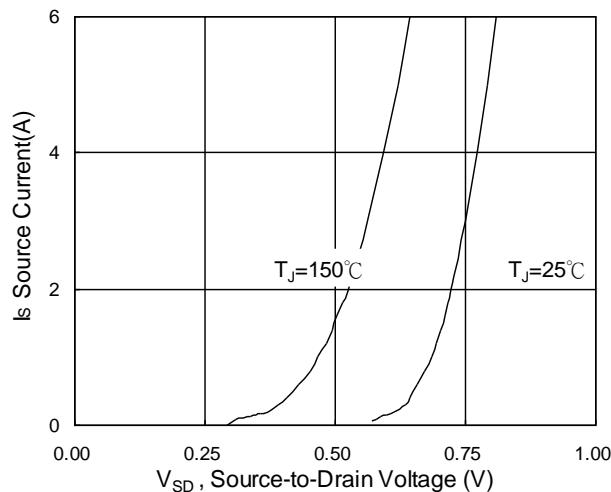


Fig.3 Forward Characteristics Of Reverse

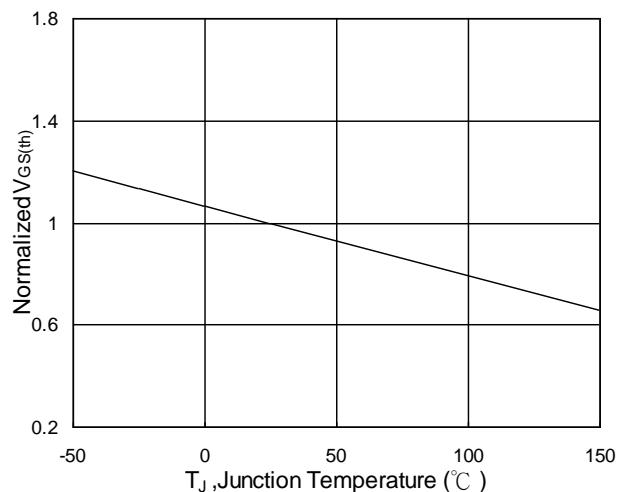


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

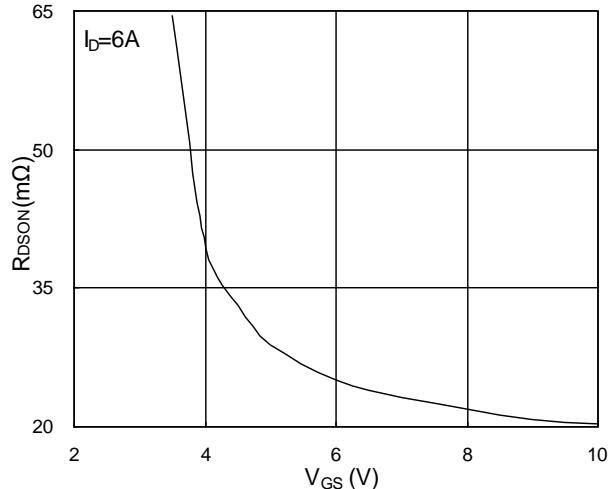


Fig.2 On-Resistance vs. Gate-Source

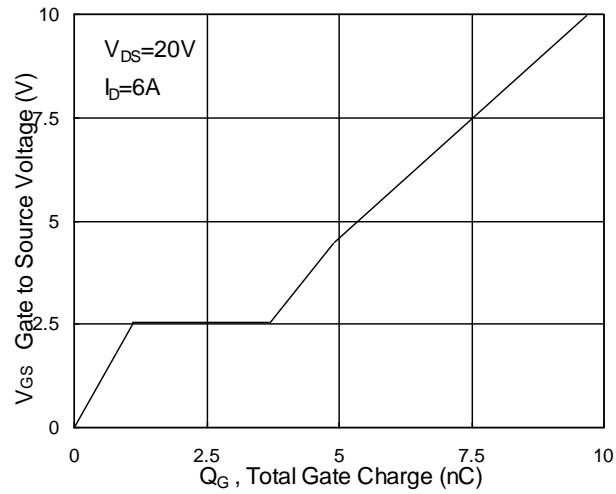


Fig.4 Gate-Charge Characteristics

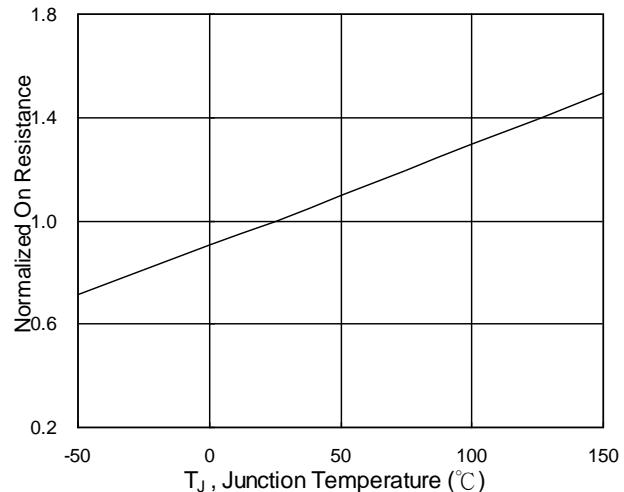


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

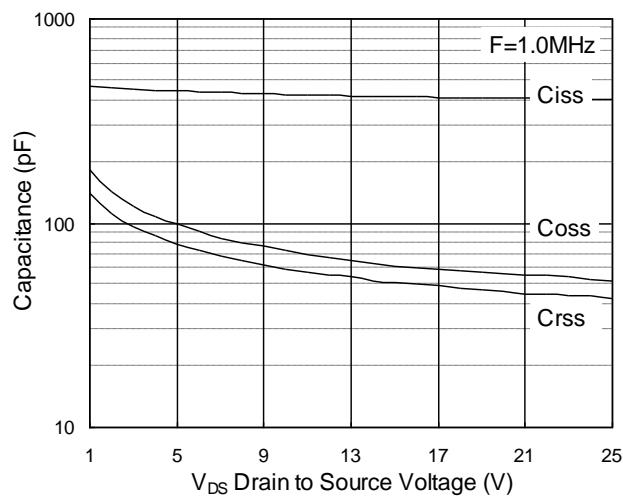


Fig.7 Capacitance

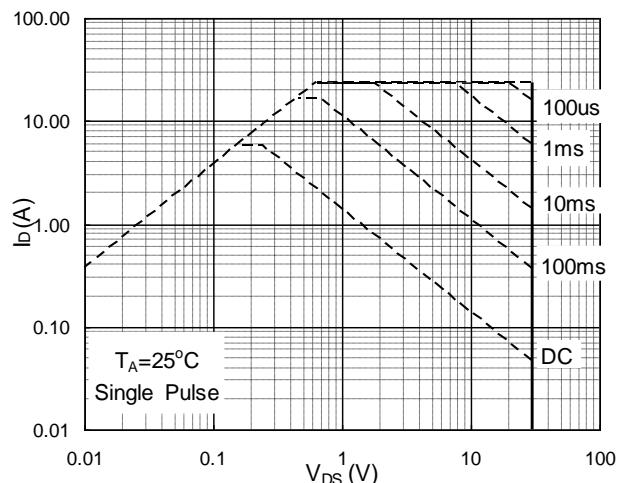


Fig.8 Safe Operating Area

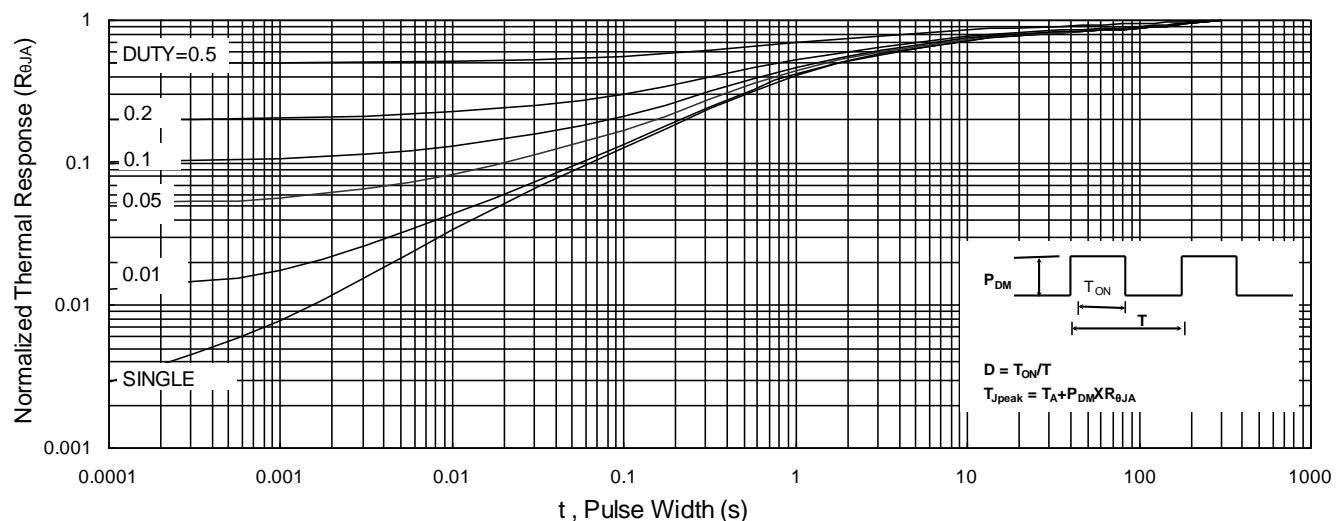


Fig.9 Normalized Maximum Transient Thermal Impedance

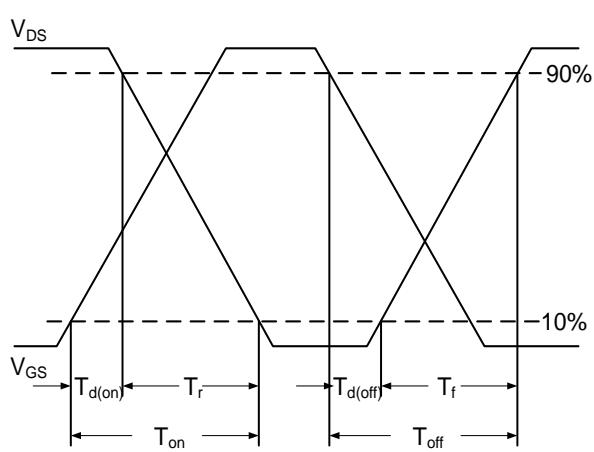


Fig.10 Switching Time Waveform

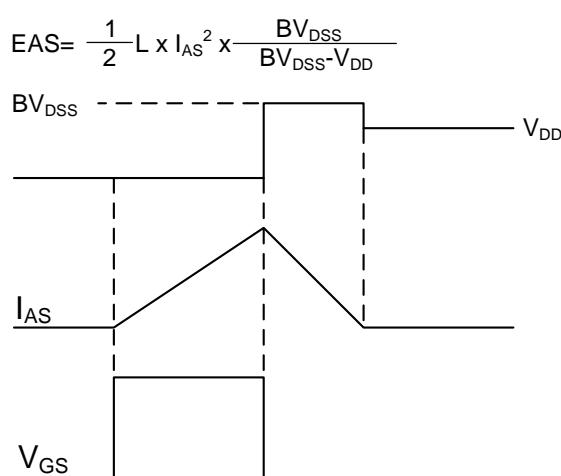


Fig.11 Unclamped Inductive Switching



P-Channel Typical Characteristics

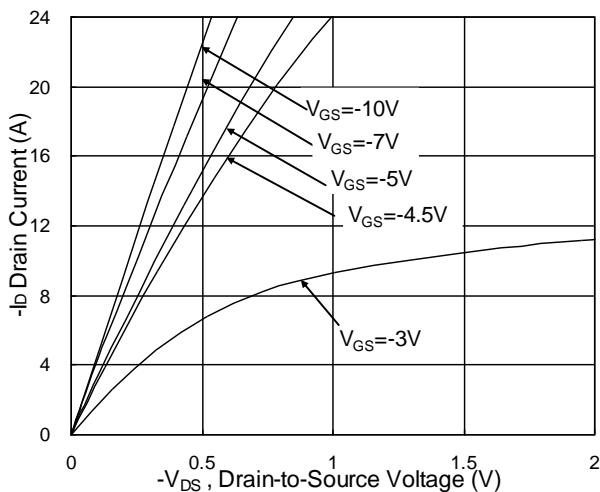


Fig.1 Typical Output Characteristics

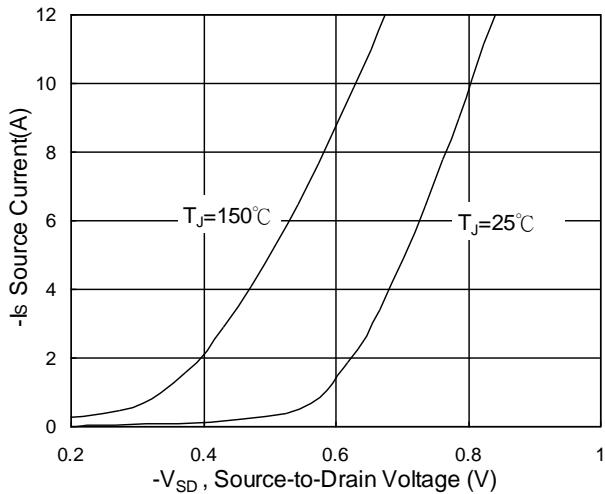


Fig.3 Forward Characteristics Of Reverse

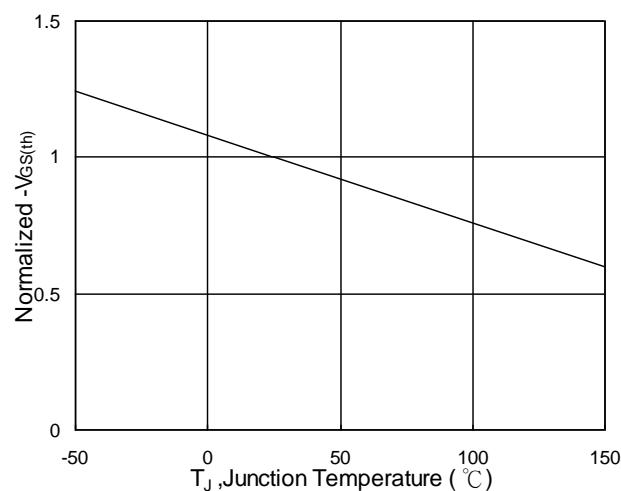


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

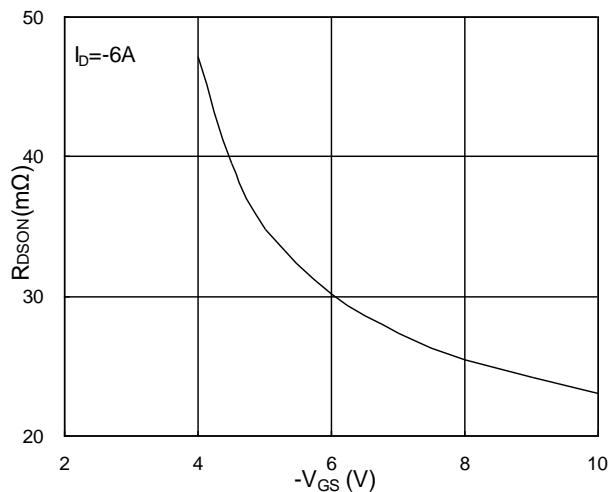


Fig.2 On-Resistance v.s Gate-Source

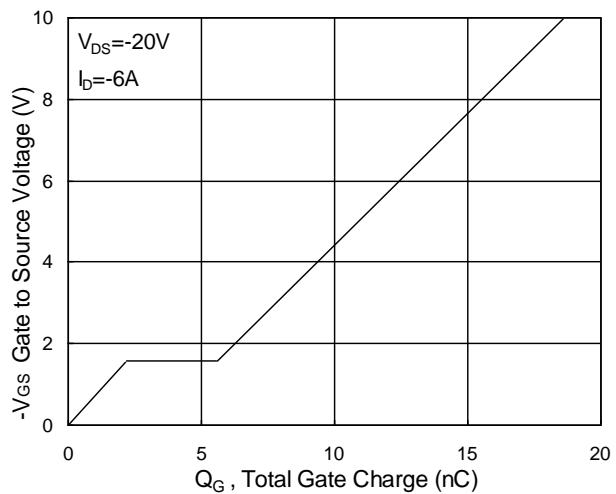


Fig.4 Gate-Charge Characteristics

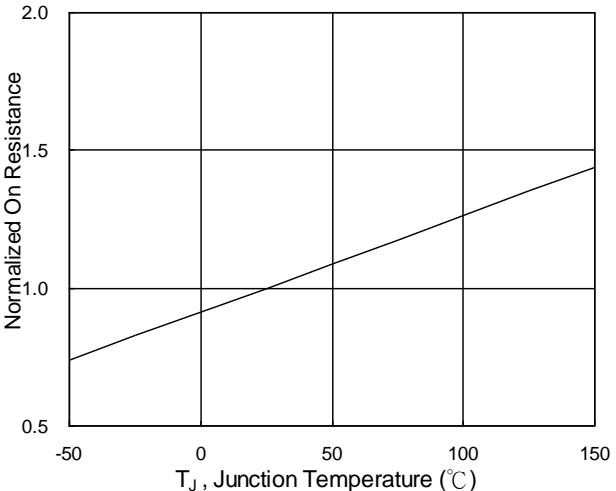


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

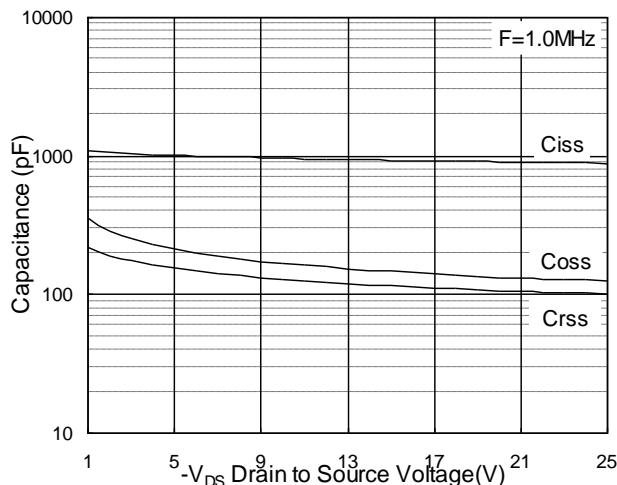


Fig.7 Capacitance

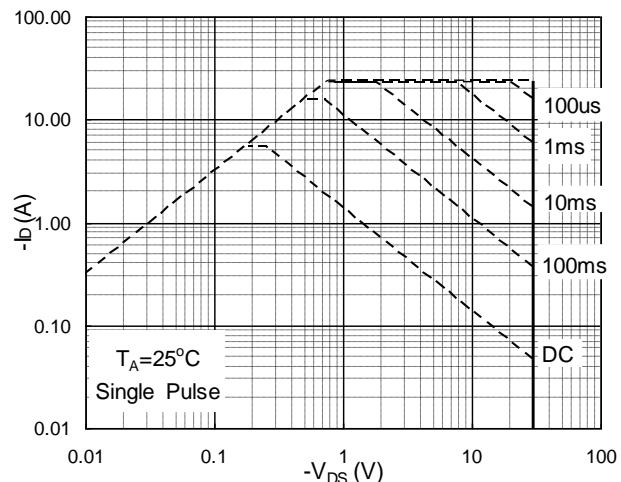


Fig.8 Safe Operating Area

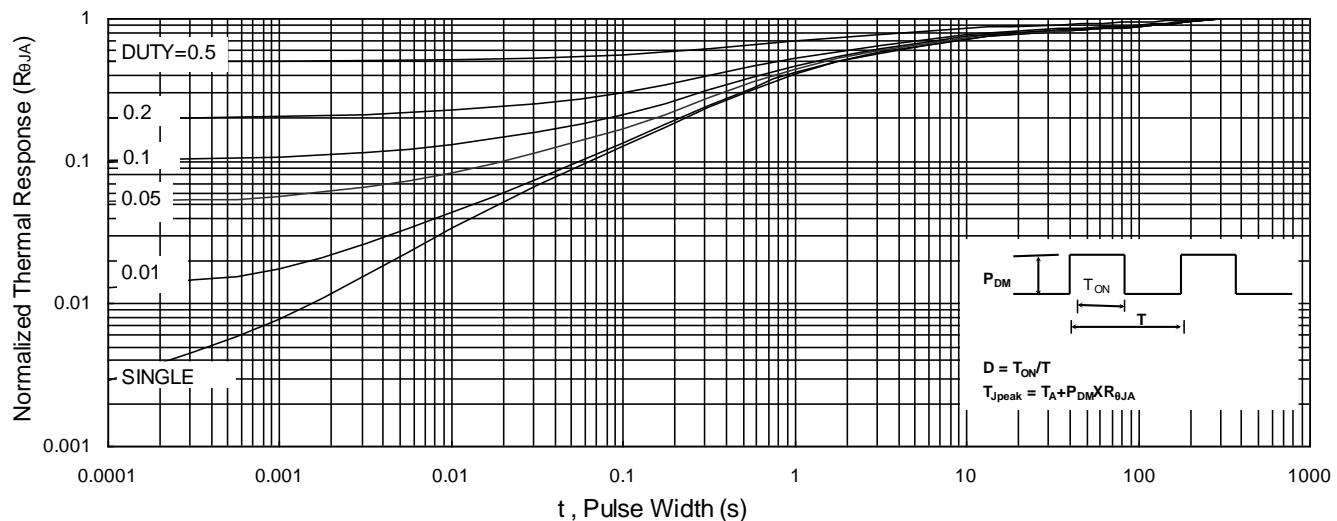


Fig.9 Normalized Maximum Transient Thermal Impedance

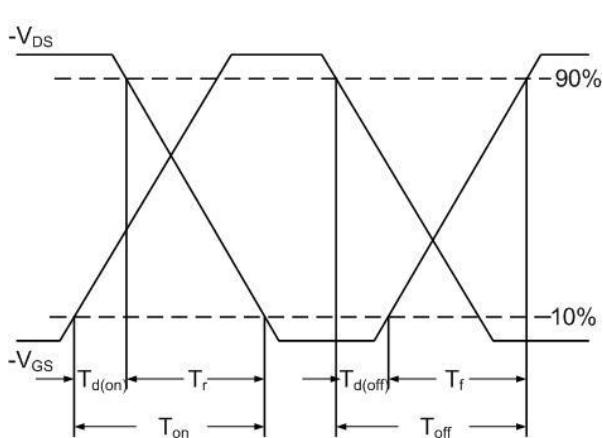


Fig.10 Switching Time Waveform

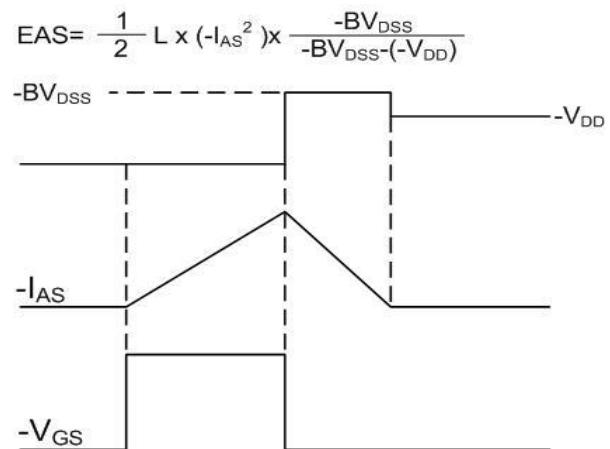


Fig.11 Unclamped Inductive Switching