HUASHUO SEMICONDUCTOR

# HSO2726

## Dual N-ch 20V Fast Switching MOSFETs

### Description

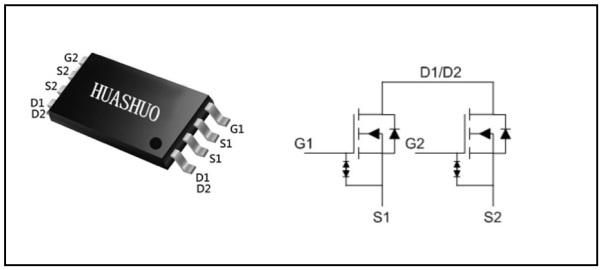
The HSO2726 is the low RDSON trenched N-CH MOSFETs with robust ESD protection. This product is suitable for Lithium-ion battery pack applications.
The HSO2726 meet the RoHS and Green Product requirement with full function reliability approved.

- Green Device Available
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology

### Product Summary

| | | |
|---|---|---|
| $V_{DS}$ | 20 | V |
| $R_{DS(ON),max}$ | 14.5 | mΩ |
| $I_D$ | 7 | A |

### TSSOP8 Pin Configuration




### Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 20 | V |
| $V_{GS}$ | Gate-Source Voltage | ±12 | V |
| $I_D$@$T_A$=25°C | Continuous Drain Current[1] | 7 | A |
| $I_D$@$T_A$=70°C | Continuous Drain Current[1] | 5.6 | A |
| $I_{DM}$ | Pulsed Drain Current[2] | 80 | A |
| $P_D$@$T_A$=25°C | Total Power Dissipation[3] | 2 | W |
| $T_{STG}$ | Storage Temperature Range | -55 to 150 | °C |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | °C |

### Thermal Data

| Symbol | Parameter | Typ. | Max. | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance Junction-ambient [1] | --- | 62.5 | °C/W |

## Electrical Characteristics ($T_J$=25 ℃, unless otherwise noted)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V , $I_D$=250uA | 20 | --- | --- | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance[2] | $V_{GS}$=4.5V , $I_D$=3.5A | 10 | 12 | 14.5 | mΩ |
| | | $V_{GS}$=4.0V , $I_D$=3.5A | 10.5 | 12.5 | 15 | |
| | | $V_{GS}$=3.7V , $I_D$=3.5A | 11 | 13.5 | 17 | |
| | | $V_{GS}$=3.1V , $I_D$=3.5A | 12 | 14 | 19.5 | |
| | | $V_{GS}$=2.5V , $I_D$=3.5A | 13 | 16 | 23 | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$=$V_{DS}$ , $I_D$ =250uA | 0.5 | --- | 1.2 | V |
| $I_{DSS}$ | Drain-Source Leakage Current | $V_{DS}$=16V , $V_{GS}$=0V , $T_J$=25℃ | --- | --- | 1 | uA |
| $I_{GSS}$ | Gate-Source Leakage Current | $V_{GS}$=±8V , $V_{DS}$=0V | --- | --- | ±10 | uA |
| gfs | Forward Transconductance | $V_{DS}$=5V , $I_D$=3.5A | --- | 21 | --- | S |
| $Q_g$ | Total Gate Charge (4.5V) | $V_{DS}$=15V , $V_{GS}$=4.5V , $I_D$=7A | --- | 11.2 | --- | nC |
| $Q_{gs}$ | Gate-Source Charge | | --- | 1.6 | --- | |
| $Q_{gd}$ | Gate-Drain Charge | | --- | 2.9 | --- | |
| $T_{d(on)}$ | Turn-On Delay Time | $V_{DD}$=10V , $V_{GS}$=4.5V , $R_G$=3Ω $I_D$=3.5A | --- | 30 | --- | ns |
| $T_r$ | Rise Time | | --- | 250 | --- | |
| $T_{d(off)}$ | Turn-Off Delay Time | | --- | 450 | --- | |
| $T_f$ | Fall Time | | --- | 700 | --- | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=15V , $V_{GS}$=0V , f=1MHz | --- | 850 | --- | pF |
| $C_{oss}$ | Output Capacitance | | --- | 81 | --- | |
| $C_{rss}$ | Reverse Transfer Capacitance | | --- | 70 | --- | |

## Diode Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current[1,4] | $V_G$=$V_D$=0V , Force Current | --- | --- | 7 | A |
| $V_{SD}$ | Diode Forward Voltage[2] | $V_{GS}$=0V , $I_S$=1A , $T_J$=25℃ | --- | --- | 1.2 | V |

Note :
1.The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The power dissipation is limited by 150℃ junction temperature
4.The data is theoretically the same as $I_D$ and $I_{DM}$ , in real applications , should be limited by total power dissipation.

## Typical Characteristics

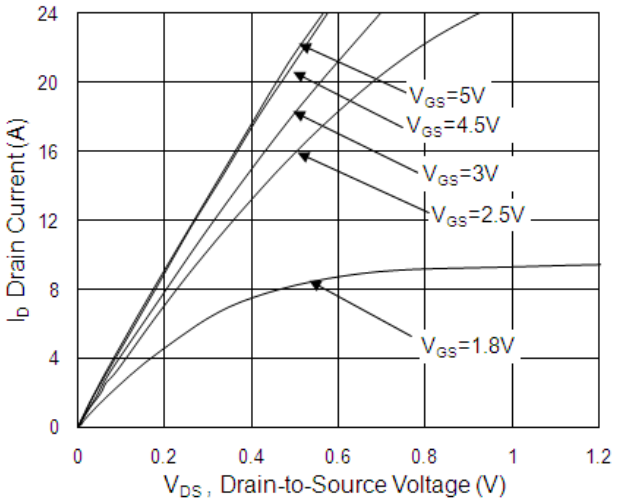



**Fig.1 Typical Output Characteristics**

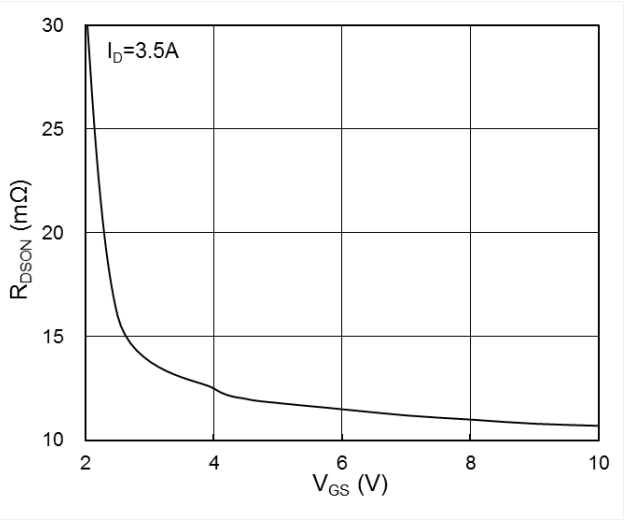



**Fig.2 On-Resistance vs. Gate-Source**

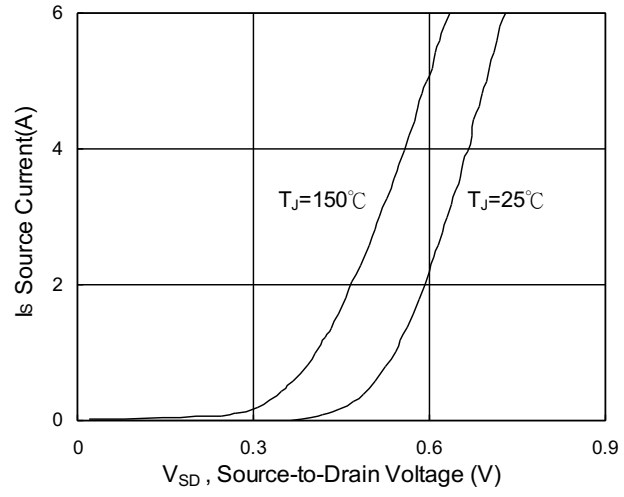



**Fig.3 Forward Characteristics of Reverse**

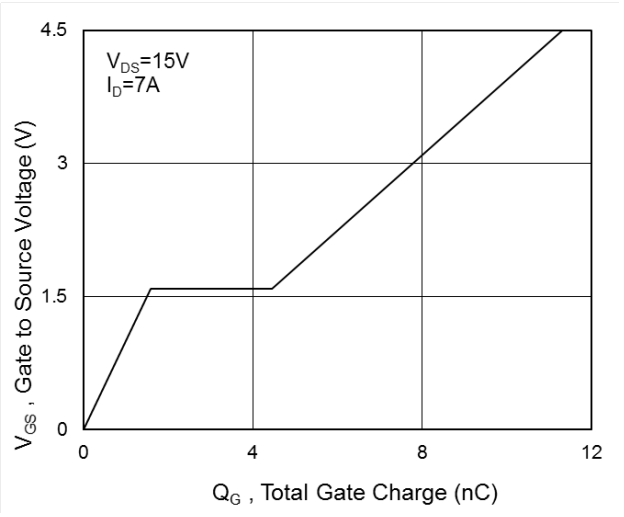



**Fig.4 Gate-Charge Characteristics**

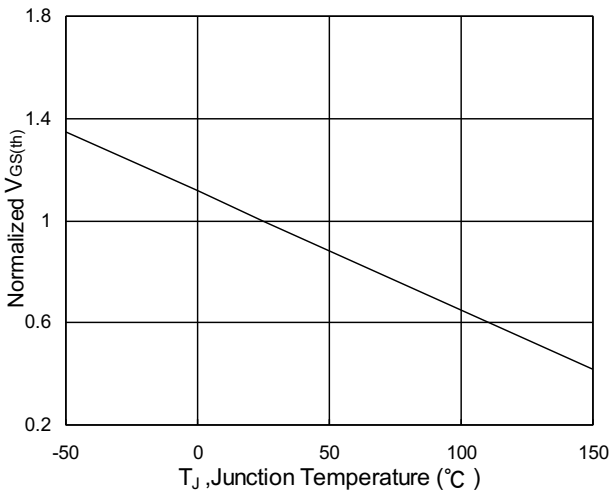



**Fig.5 $V_{GS(th)}$ vs. $T_J$**

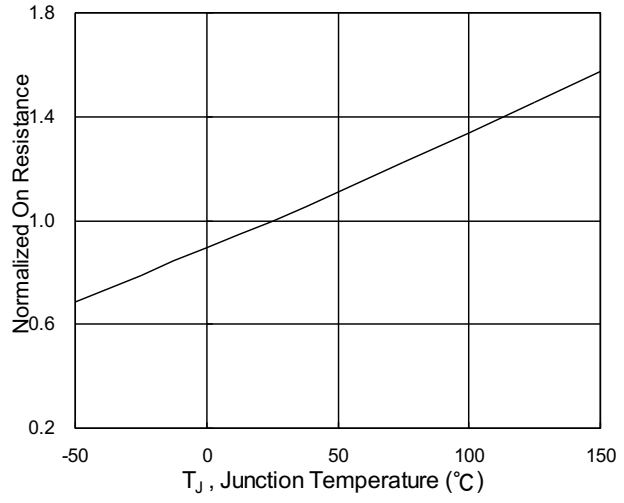



**Fig.6 Normalized $R_{DSON}$ vs. $T_J$**

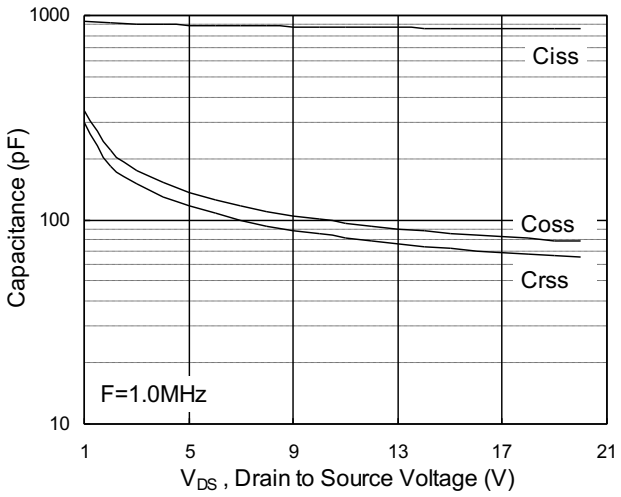



Fig.7 Capacitance

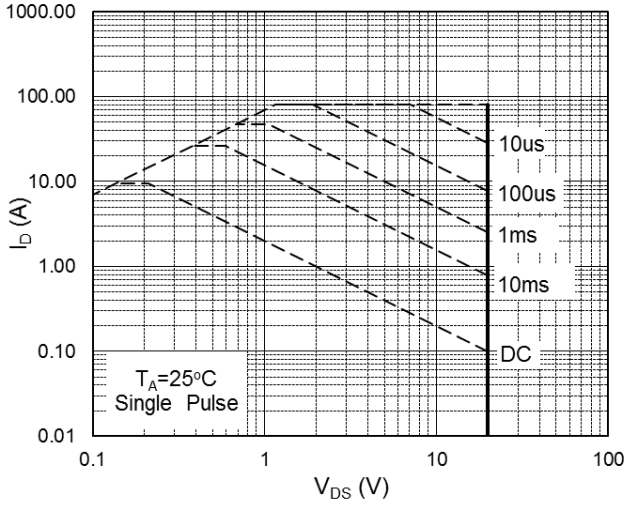



Fig.8 Safe Operating Area

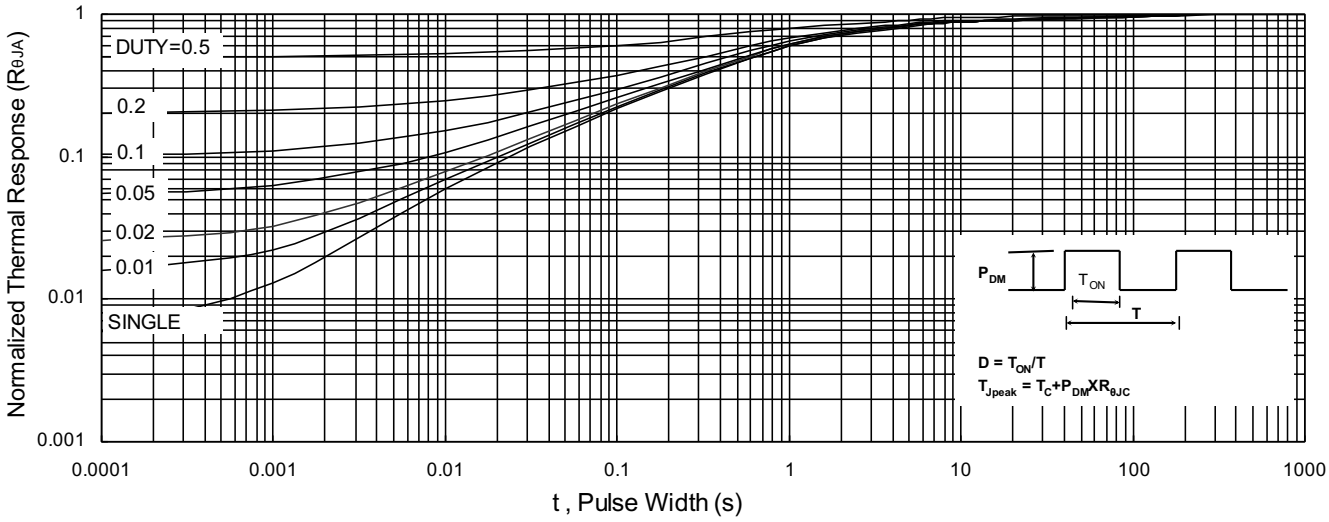



Fig.9 Normalized Maximum Transient Thermal Impedance

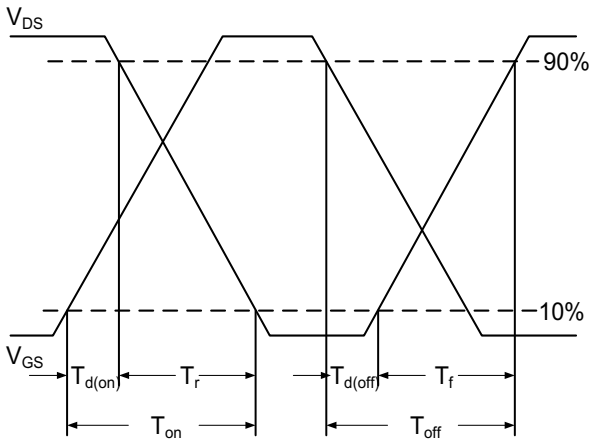



Fig.10 Switching Time Waveform

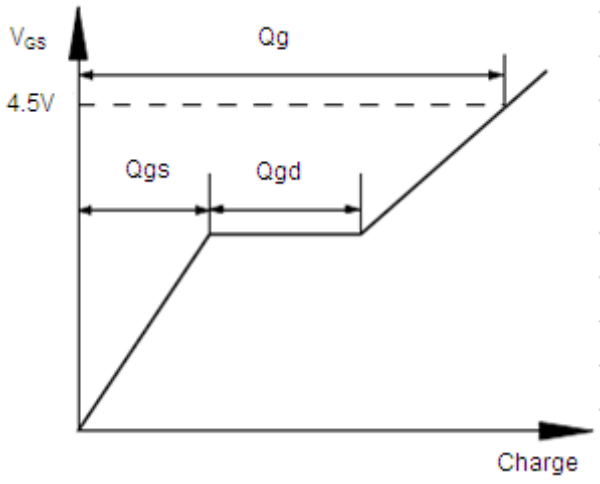
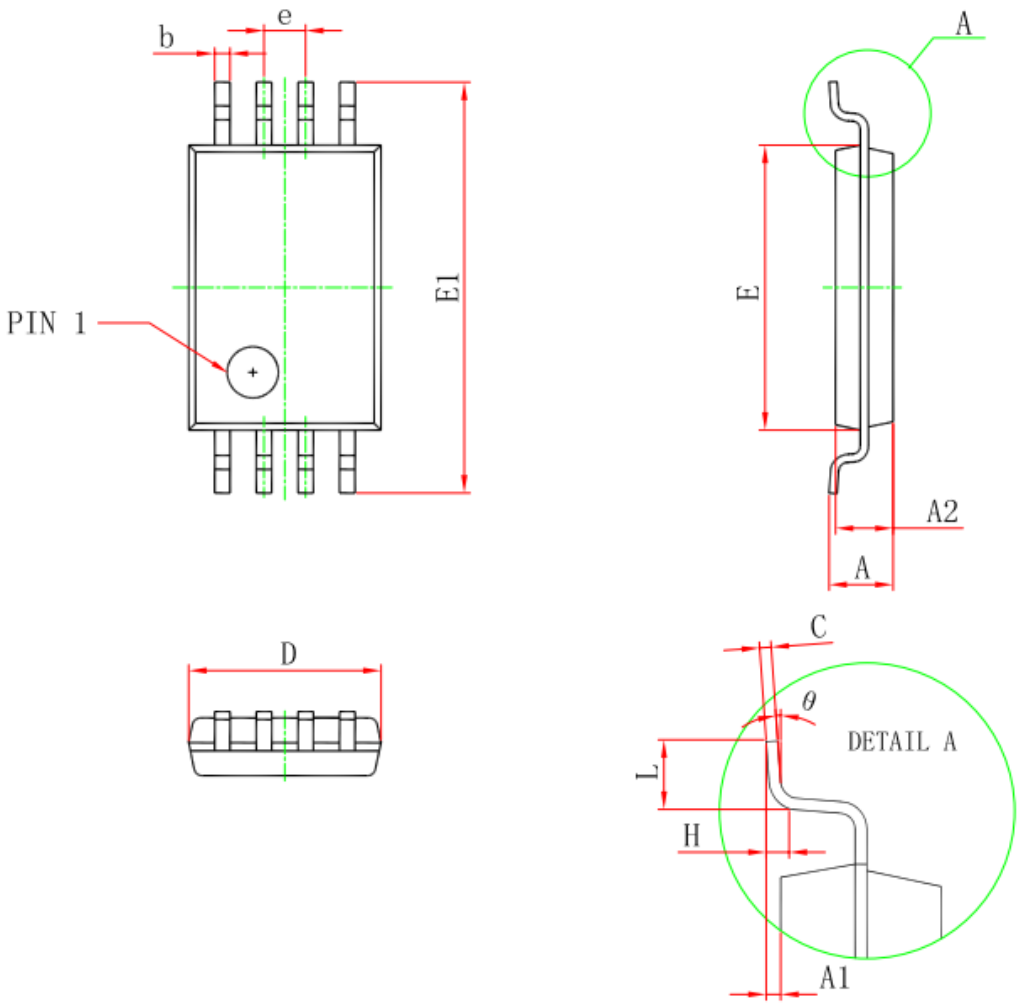



Fig.11 Gate Charge Waveform

# TSSOP8 Package Outline Dimensions




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| E | 4.300 | 4.500 | 0.169 | 0.177 |
| b | 0.190 | 0.300 | 0.007 | 0.012 |
| c | 0.090 | 0.200 | 0.004 | 0.008 |
| E1 | 6.250 | 6.550 | 0.246 | 0.258 |
| A | | 1.200 | | 0.047 |
| A2 | 0.800 | 1.000 | 0.031 | 0.039 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| e | 0.65 (BSC) | | 0.026 (BSC) | |
| L | 0.500 | 0.700 | 0.020 | 0.028 |
| H | 0.25(TYP) | | 0.01(TYP) | |
| θ | 1° | 7° | 1° | 7° |

# Marking Instruction